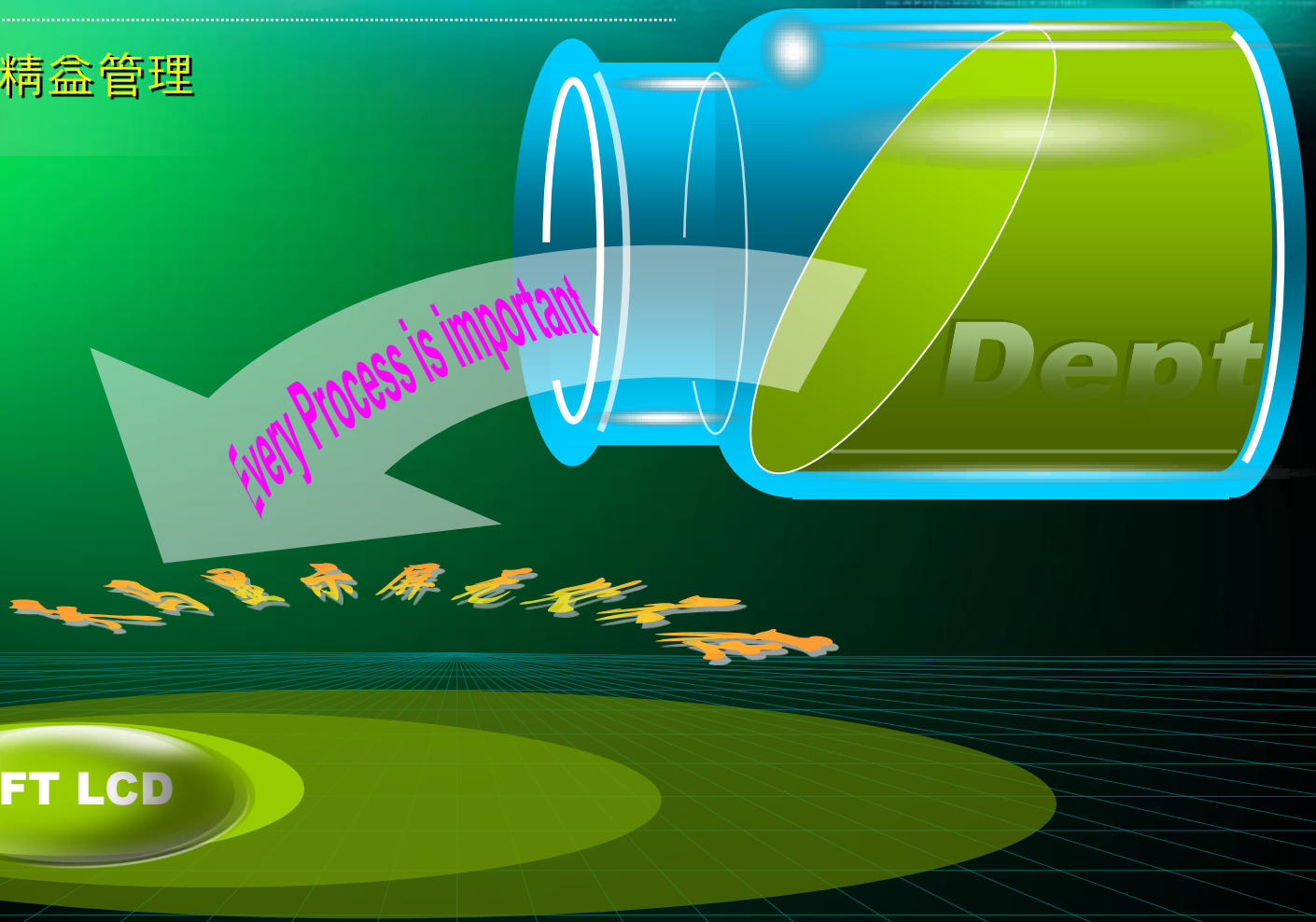
TFT-LCD 工艺制程简介

Contents

❑ Team work

客户导向，团结协作

精益生产，精益管理

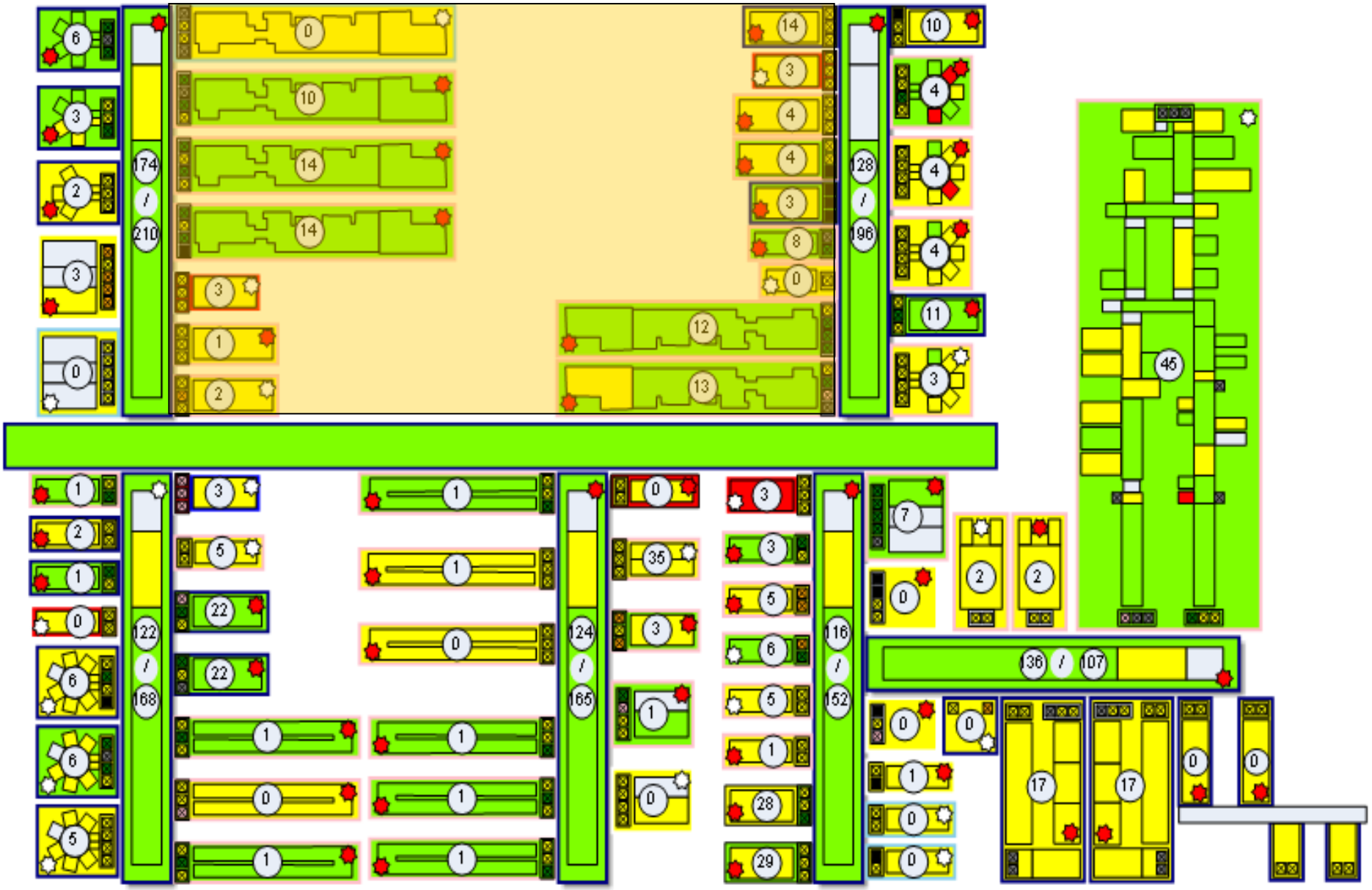


❑ TFT-LCD ENGLISH

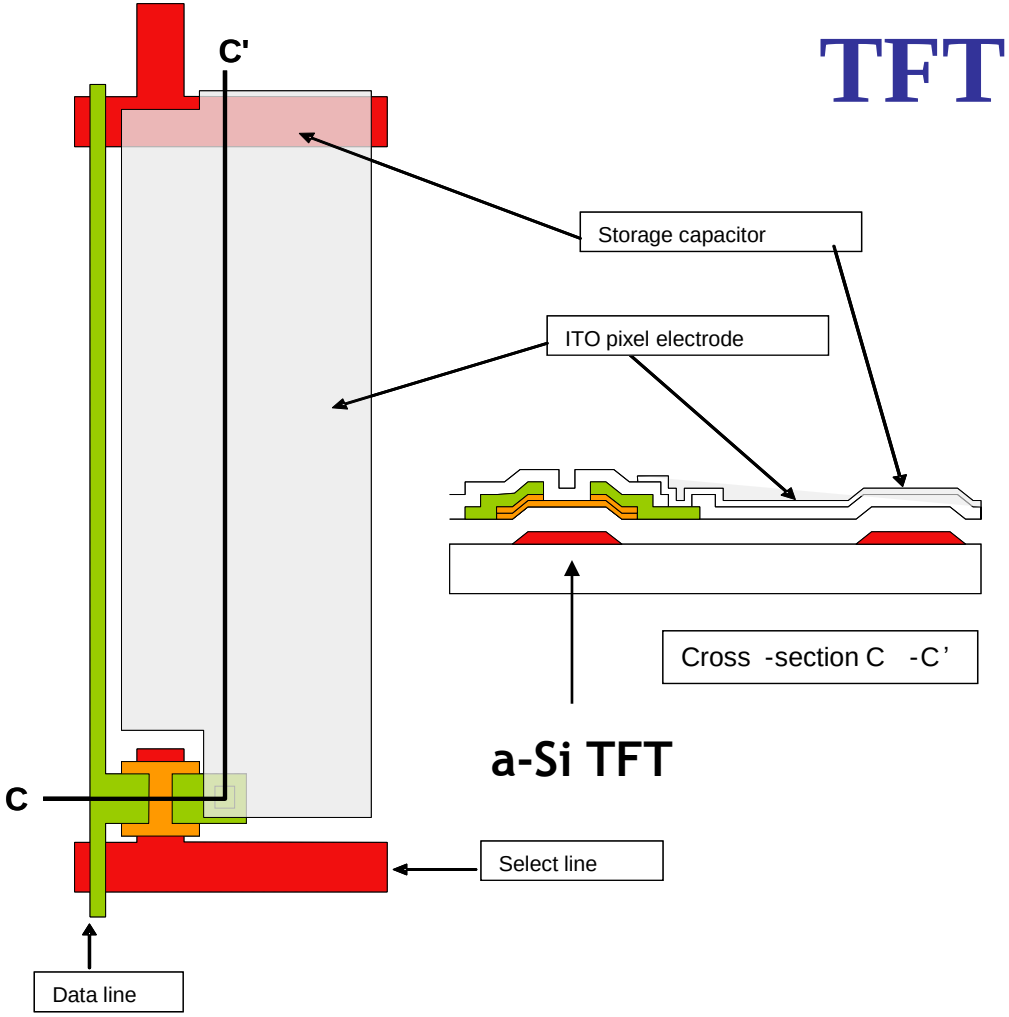
一：Array Process

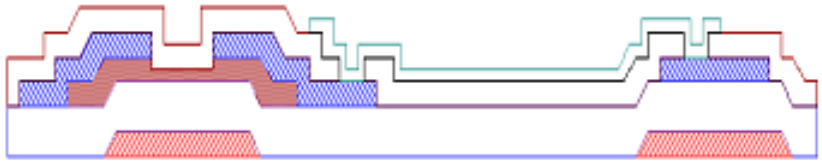
- Organization

❑ Array Layout

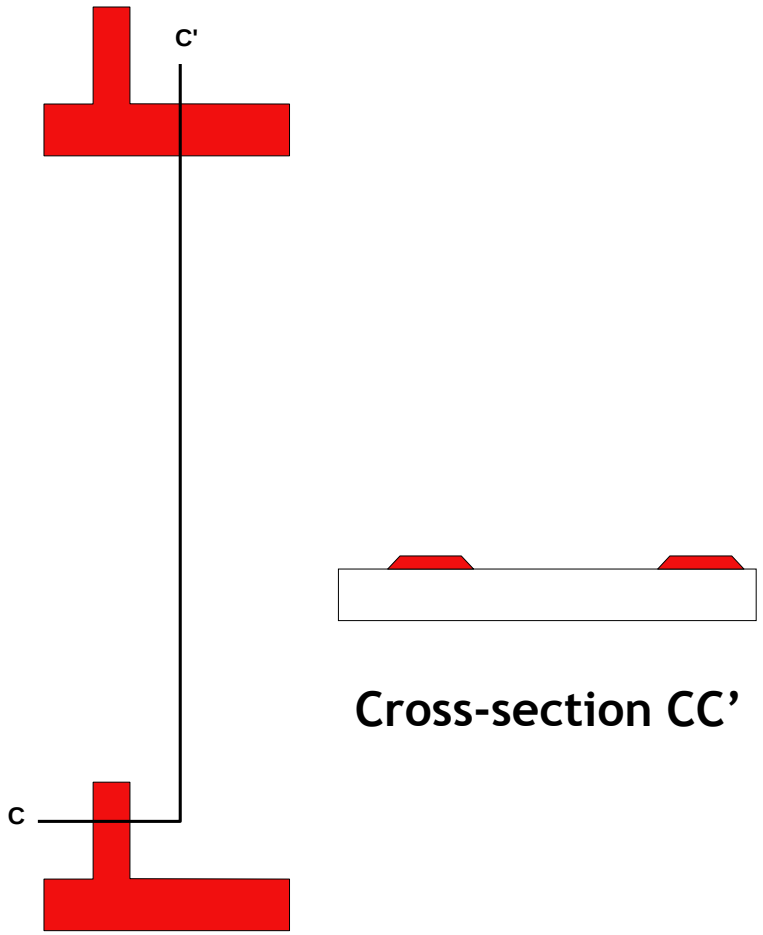


TFT Structure



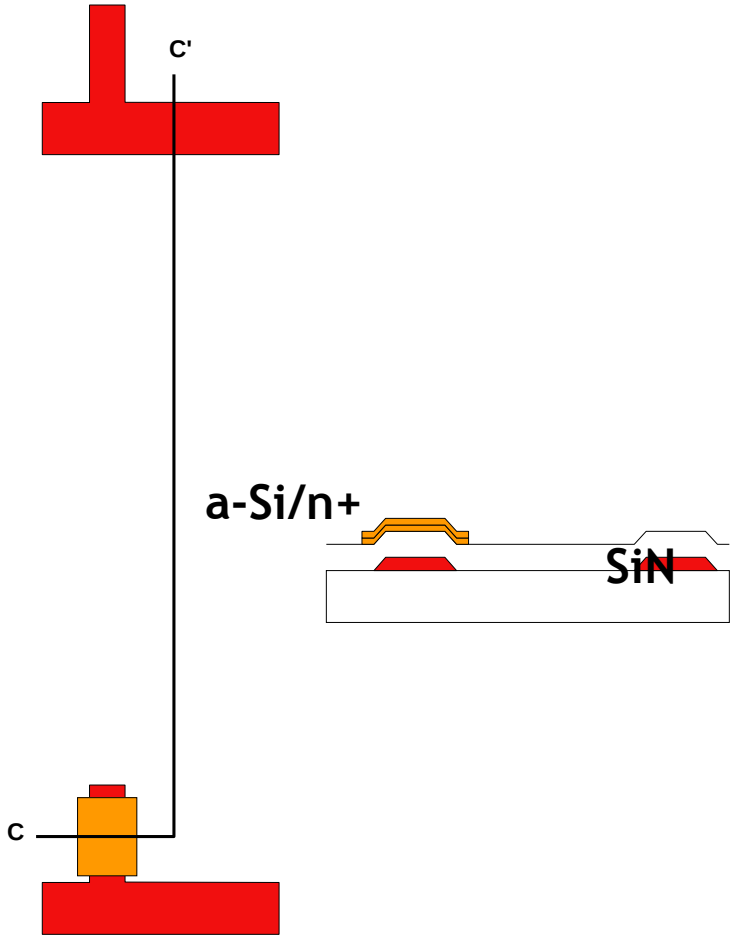


a-Si TFT array process – step 1



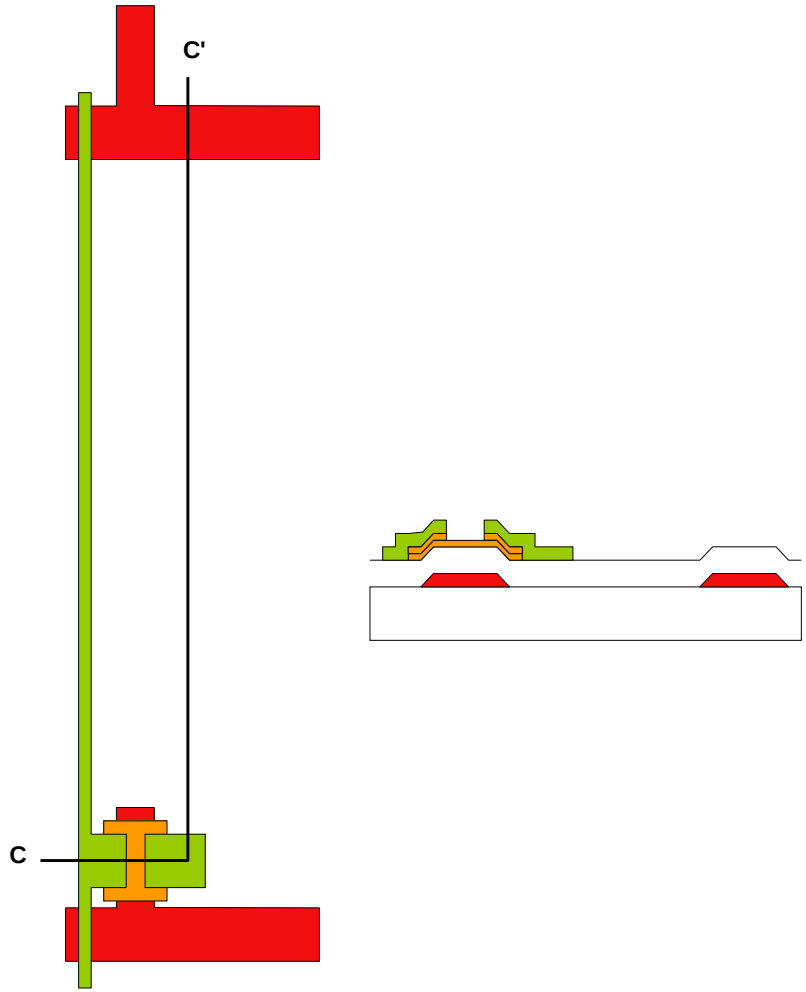
- Deposit and pattern gate metal
- Functions:
  - Gate of TFT
  - Select lines
  - Bottom electrode of storage capacitor
- Metal options:
  - Ti/Al/Ti
  - Al/Mo
  - Cr
  - Mo

a-Si TFT array process - step 2



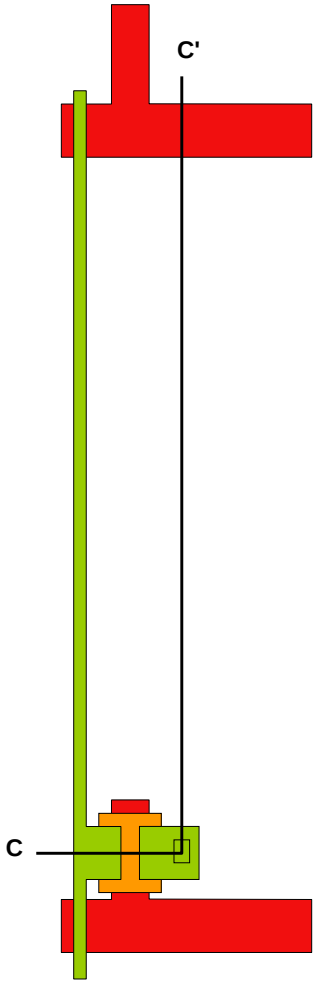
- Deposition of SiN/a-Si/n+ by PECVD, patterning of a-Si
- SiN is gate dielectric and storage capacitor dielectric
  - Selective etch of a-Si
  - SiN is not etched

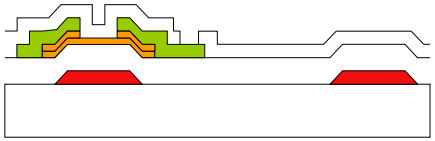
a-Si TFT array process - step 3



- Deposition and patterning of source/drain metal
- Functions:
  - Source and drain metal
  - Data line metal
- Metal options
  - Ti/Al/Ti or Ti/Al
  - Cr
  - Mo or Mo/Al

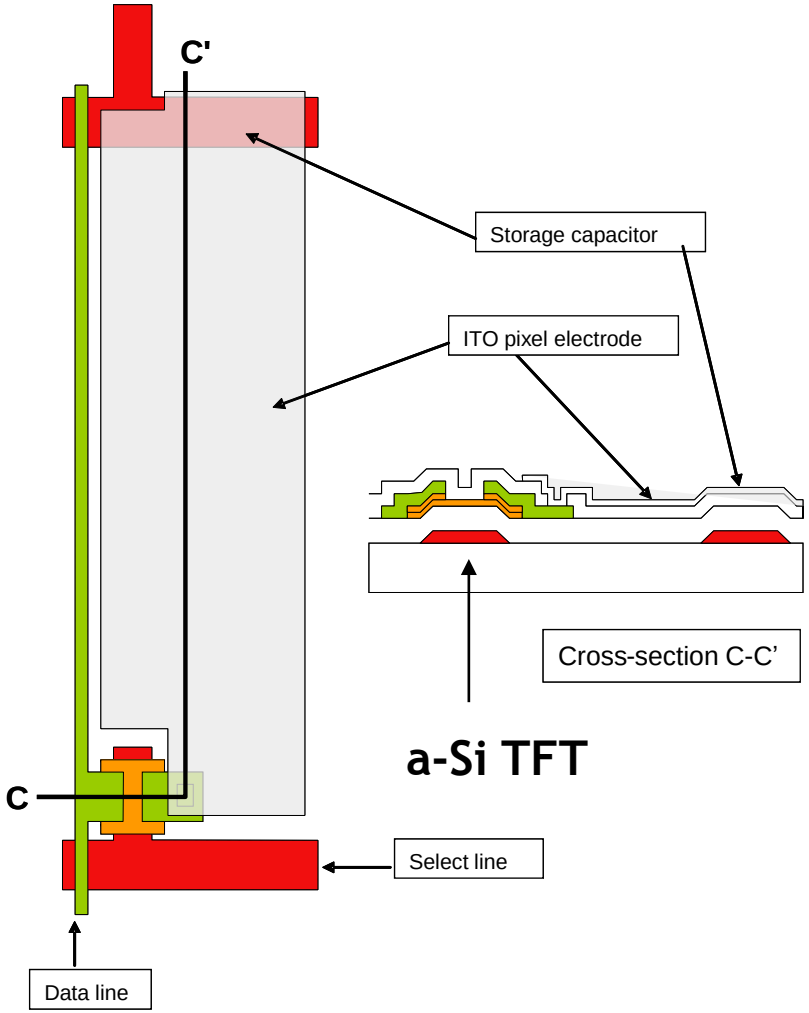
a-Si TFT array process - step 4





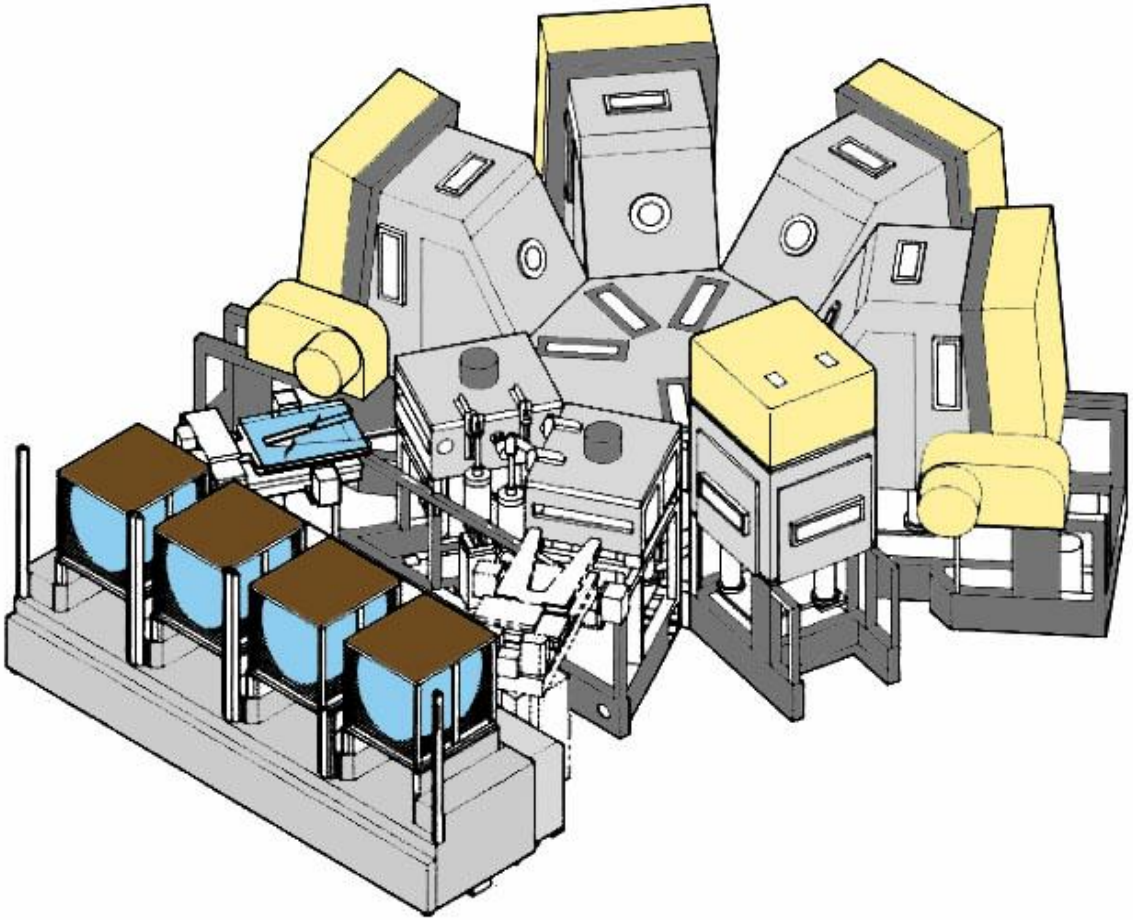
- Deposition and patterning of passivation SiN by PECVD
- Function:
  - Passivate TFT

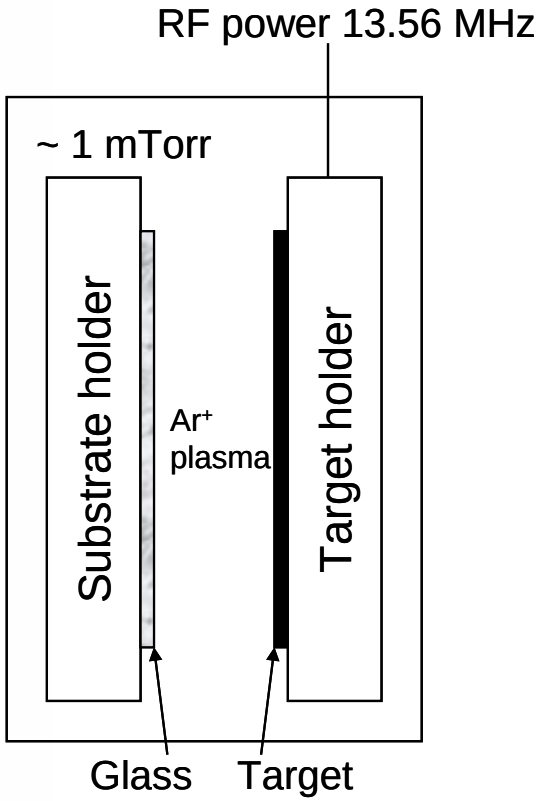
a-Si TFT array process - step 5



- Deposition and patterning of ITO
- Function:
  - Pixel electrode
  - Top electrode of storage capacitor

TFT ARRAY PROCESS___PVD/CVD



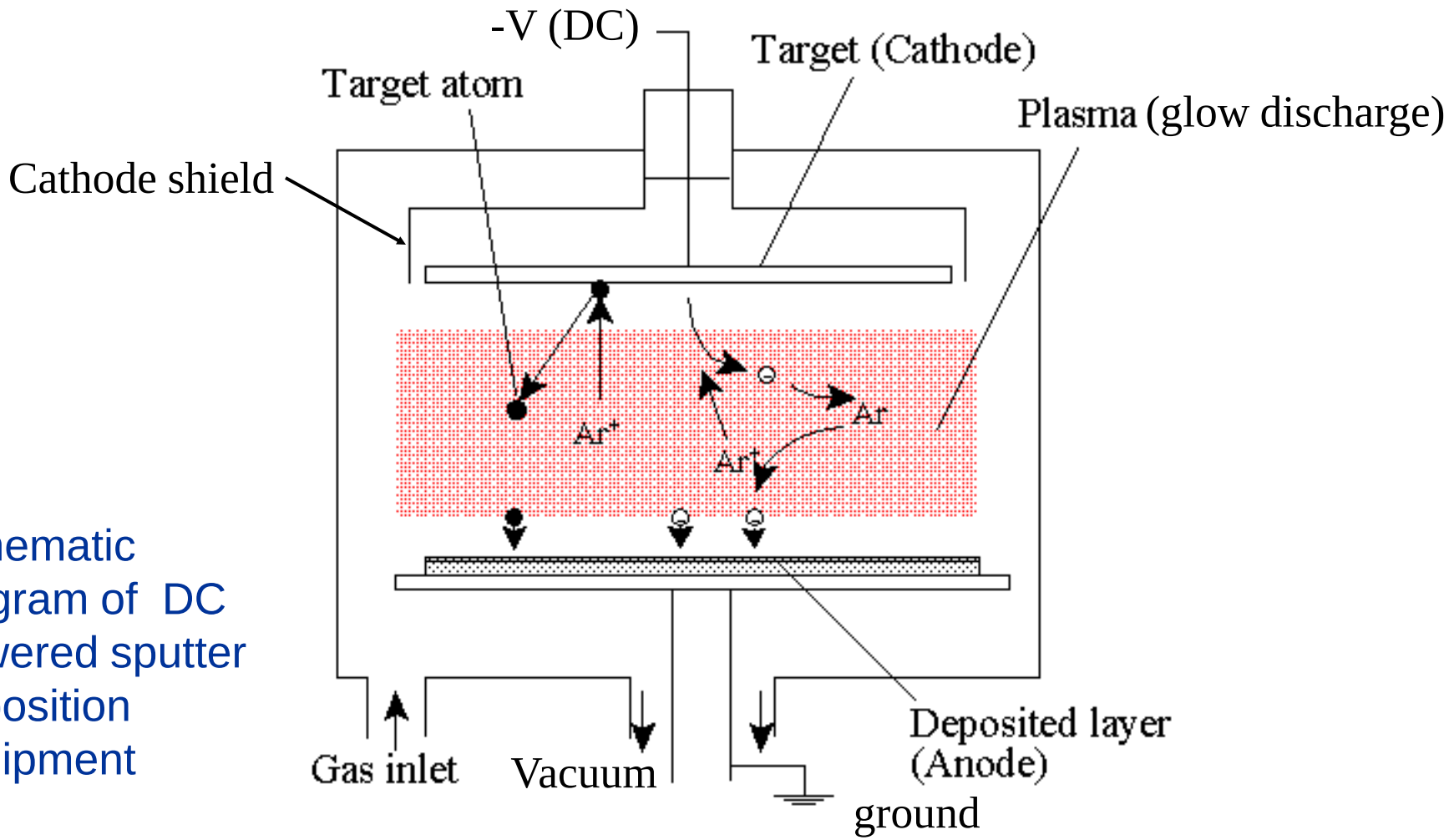


Used for ITO (Indium Tin Oxide transparent conductor) and for metals (Al, Mo, Cr, etc.)

PVD原理

DC Sputter deposition

~-100-1000V

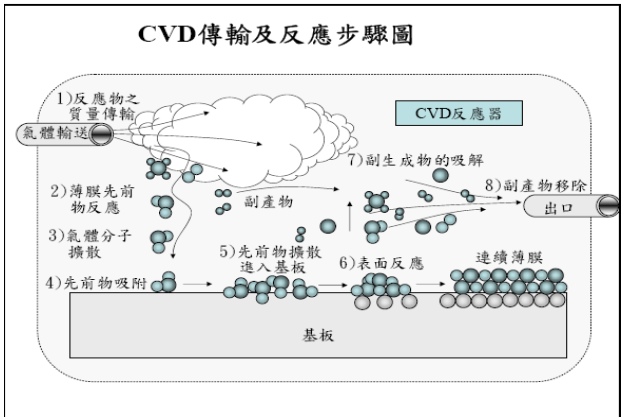


Schematic diagram of DC powered sputter deposition equipment

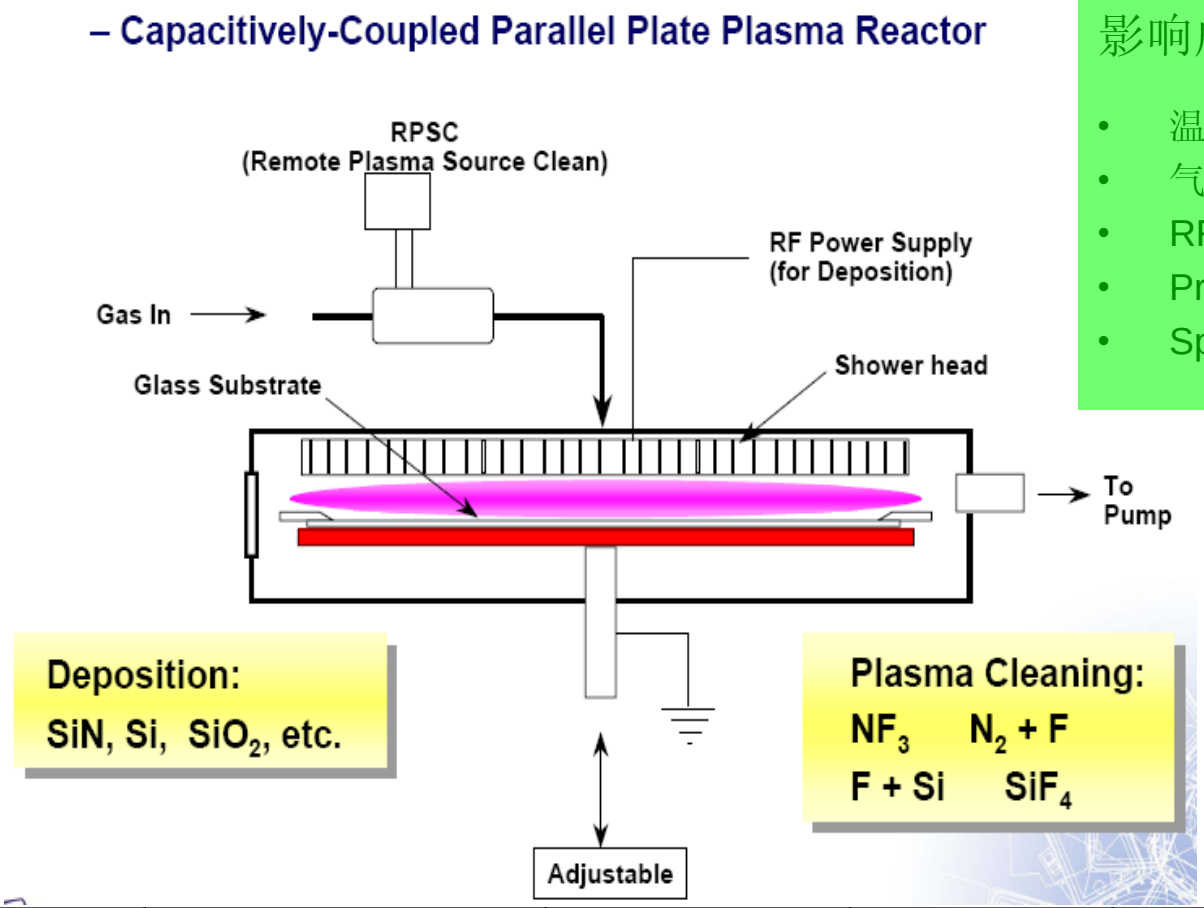
PECVD (即等离子体增强化学气相沉积)

- 工作原理:采用等离子辅助对化合物进行催化分解
- 目的: 利用等离子体辅助活化反应气体,降低反应温度,改善薄膜质量

AKT-5500



PECVD原理

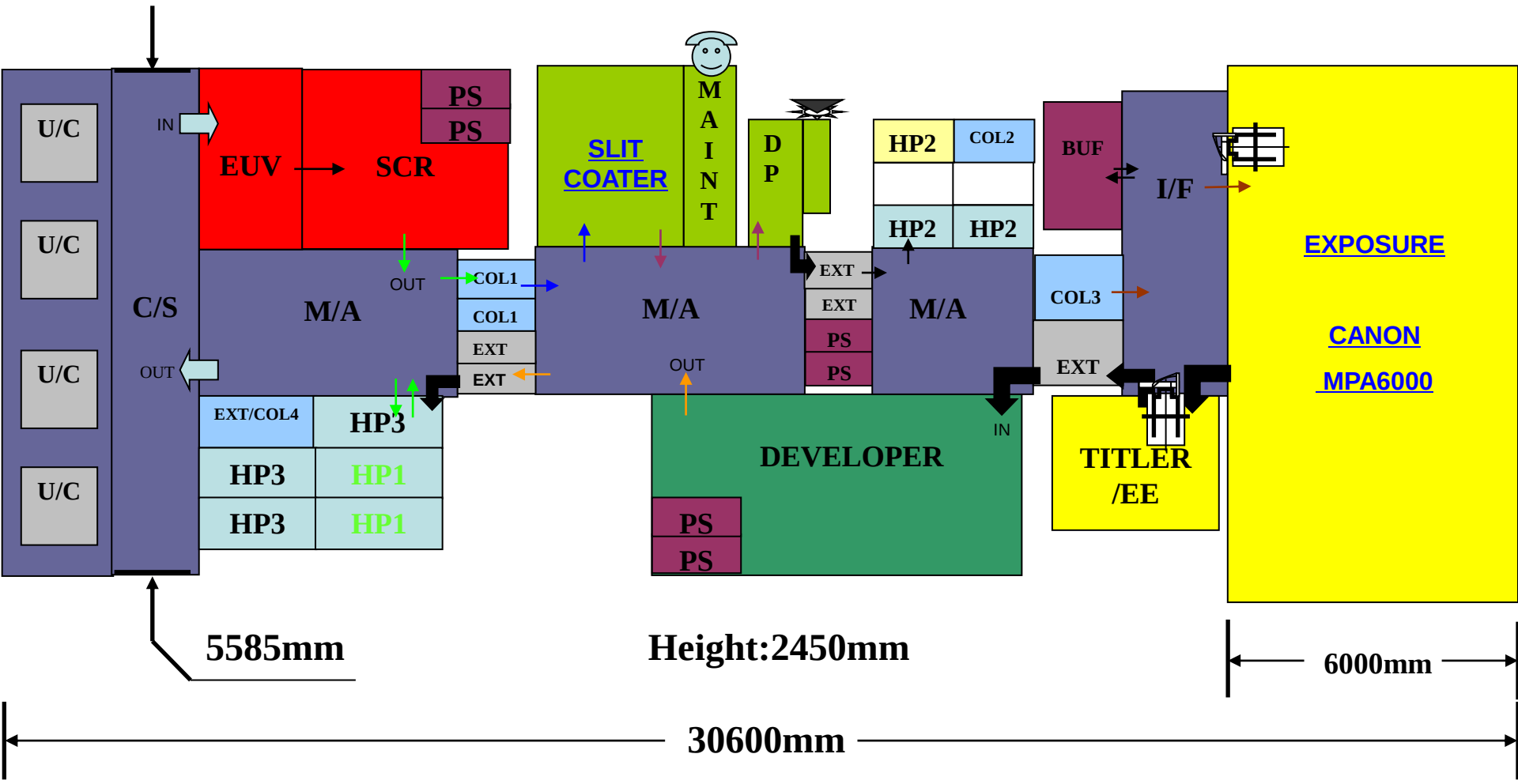


影响成膜工艺的主要参数

- 温度
- 气体流量比 (Si:H,N:H,Si:N)
- RF
- Pressure
- Spacing (上下电极间距)

Layer	Feed gas	Material	Temp	Function
3 Layer	SiH_4, N_2, NH_3	A-SiN_x	320~350℃	Gate insulator
	SiH_4, H_2	a-Si		Semiconductor
	SiH_4, PH_3, H_2	n^+ a-Si		Contact layer at source and drain
1 Layer	SiH_4, N_2, NH_3	A-SiN_x	270~290 ℃	passivation

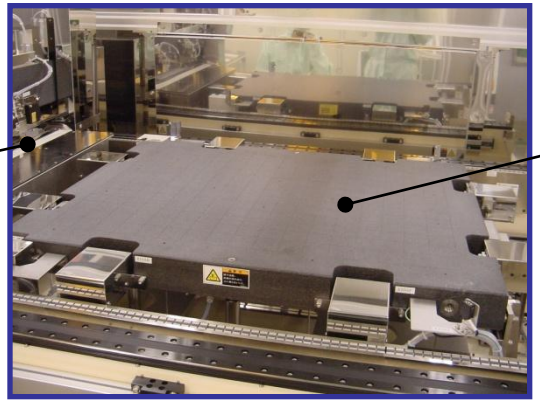
TFT ARRAY PROCESS___PHOTO



JUMP

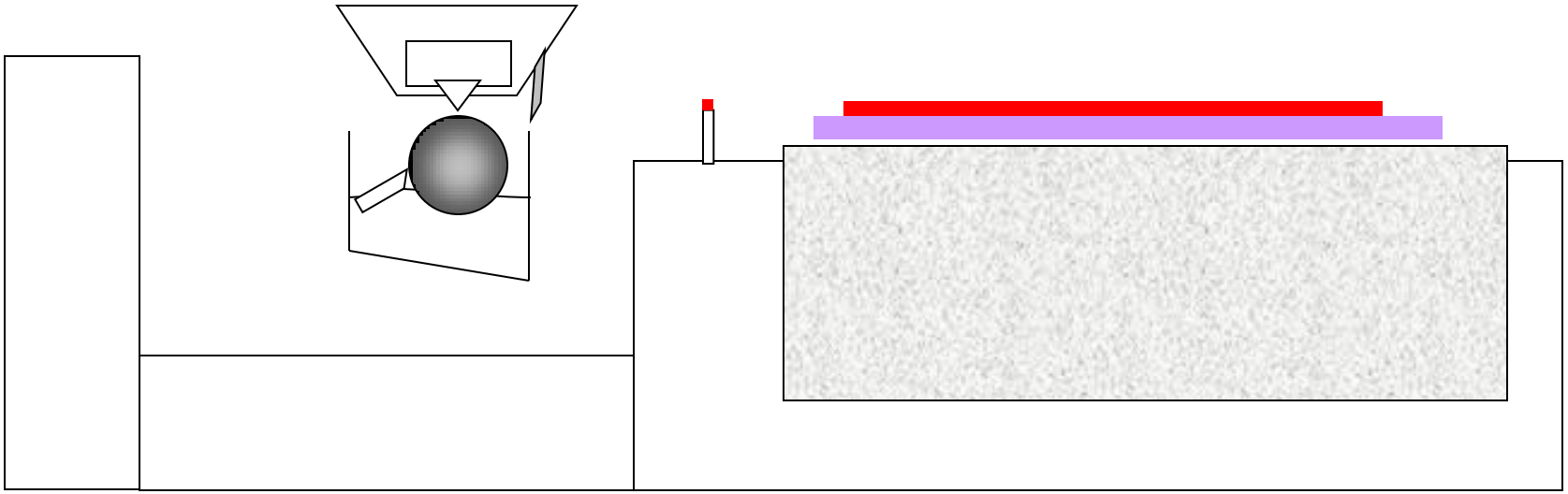
Slit Coater & DP

Nozzle

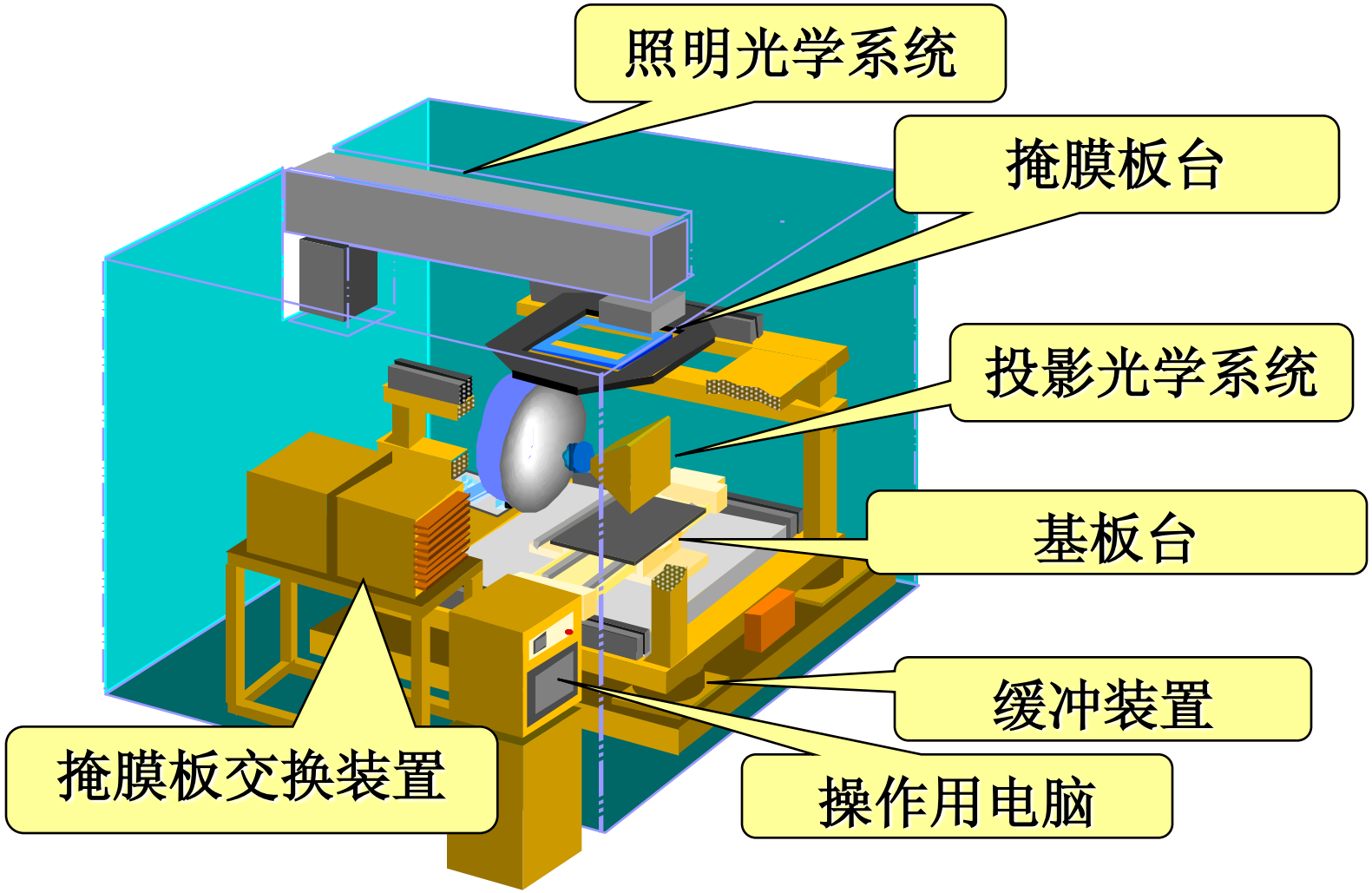


stage

DP

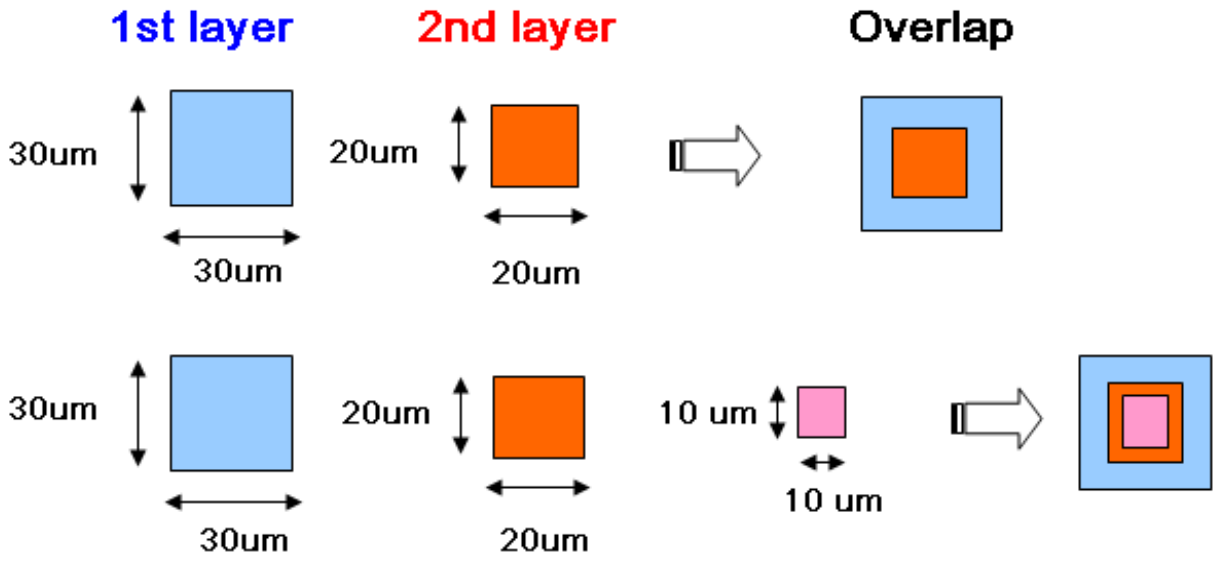


MPA6000 Exposure unit

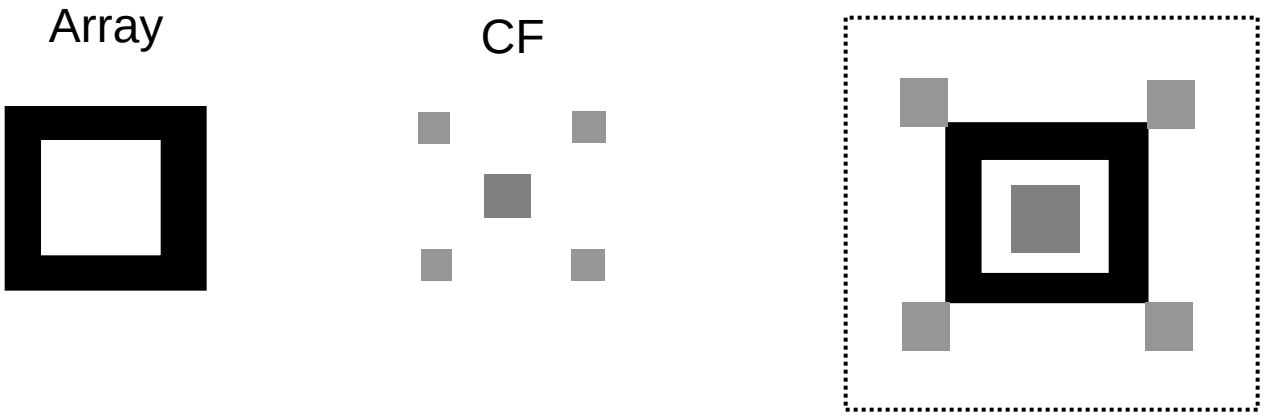


TP & OL Mark

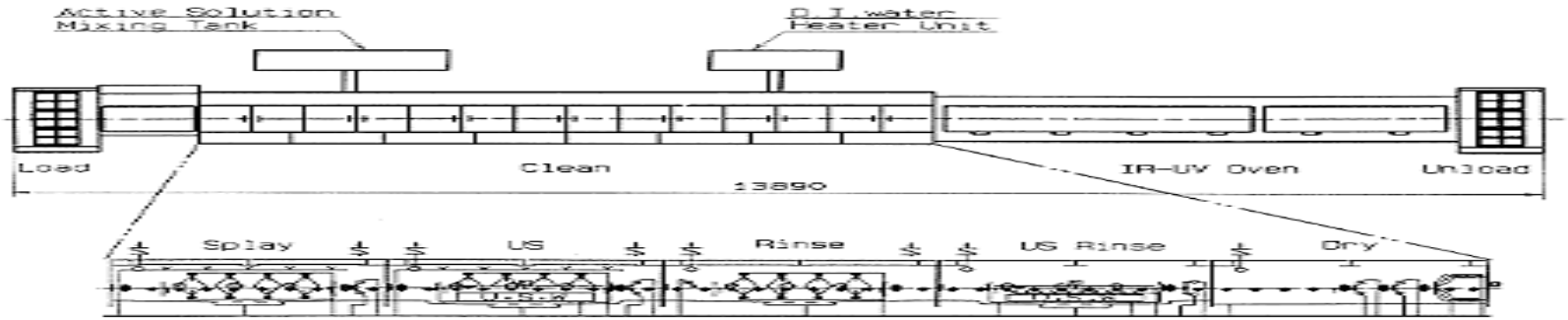
OL



TP



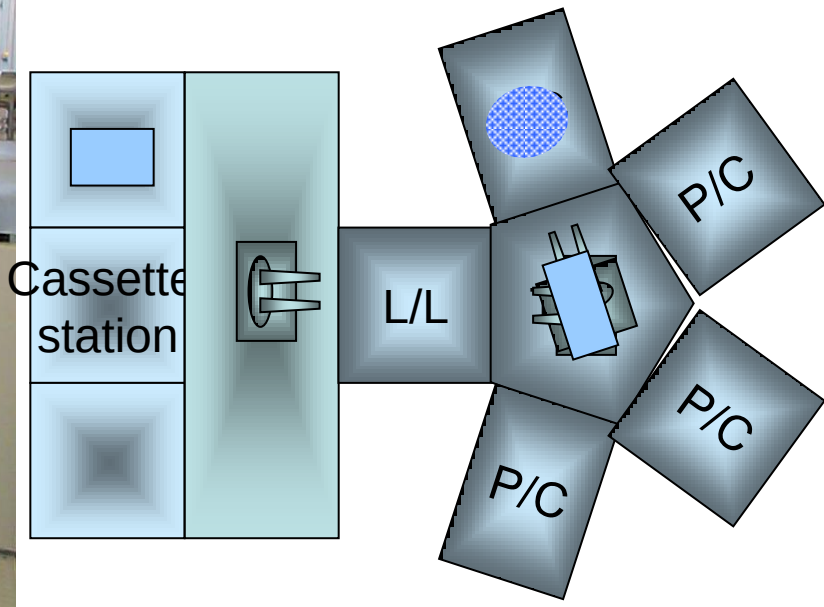
TFT ARRAY PROCESS___WET



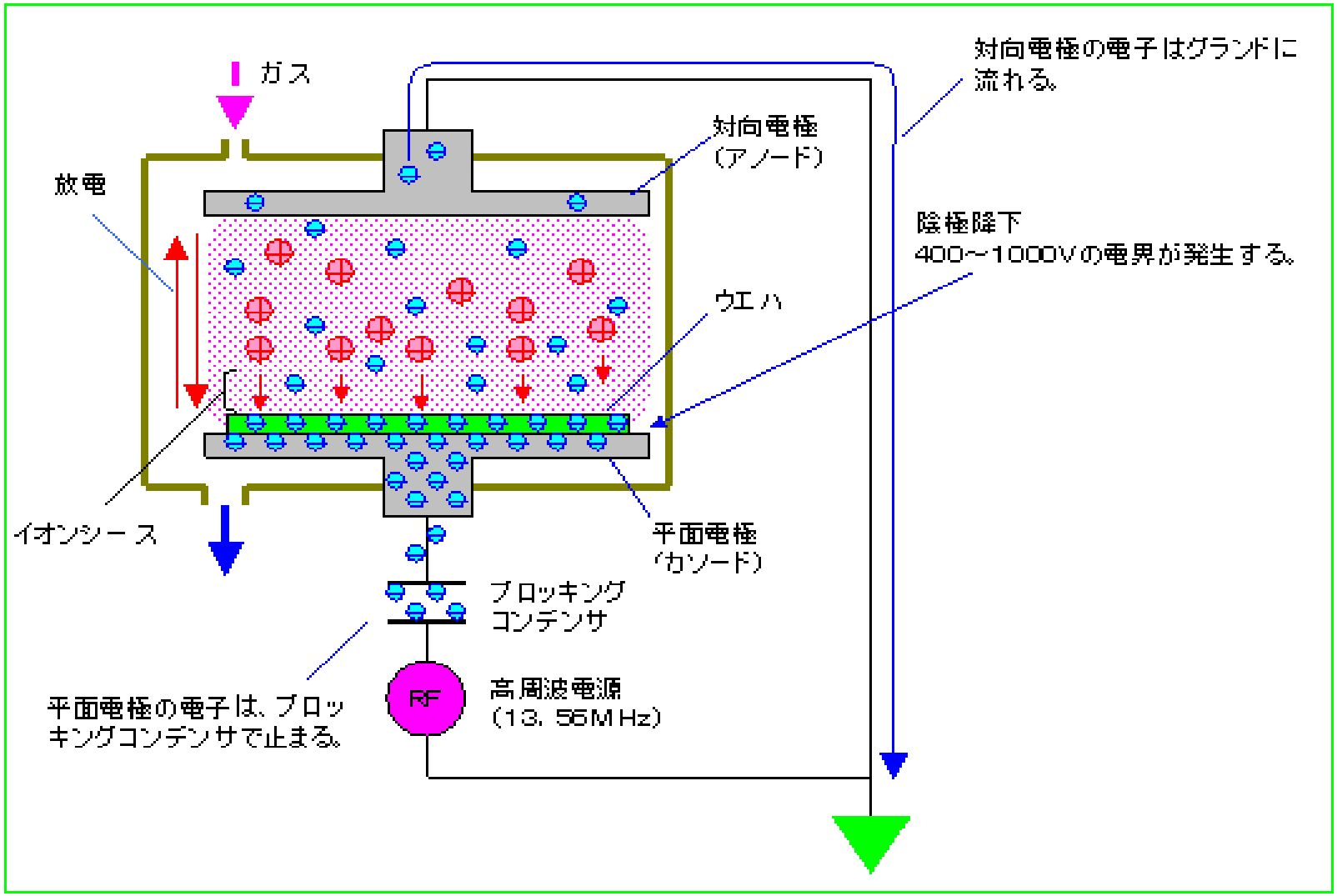
Stripper

Wet etcher

TFT ARRAY PROCESS___DRY



DET原理



RIE：指的是Reactive ion etching，即反应离子刻蚀

利用Plasma将反应气体解离，ion轰击与radicals反应将Film移除，真空下进行

EPD for Dry Etching

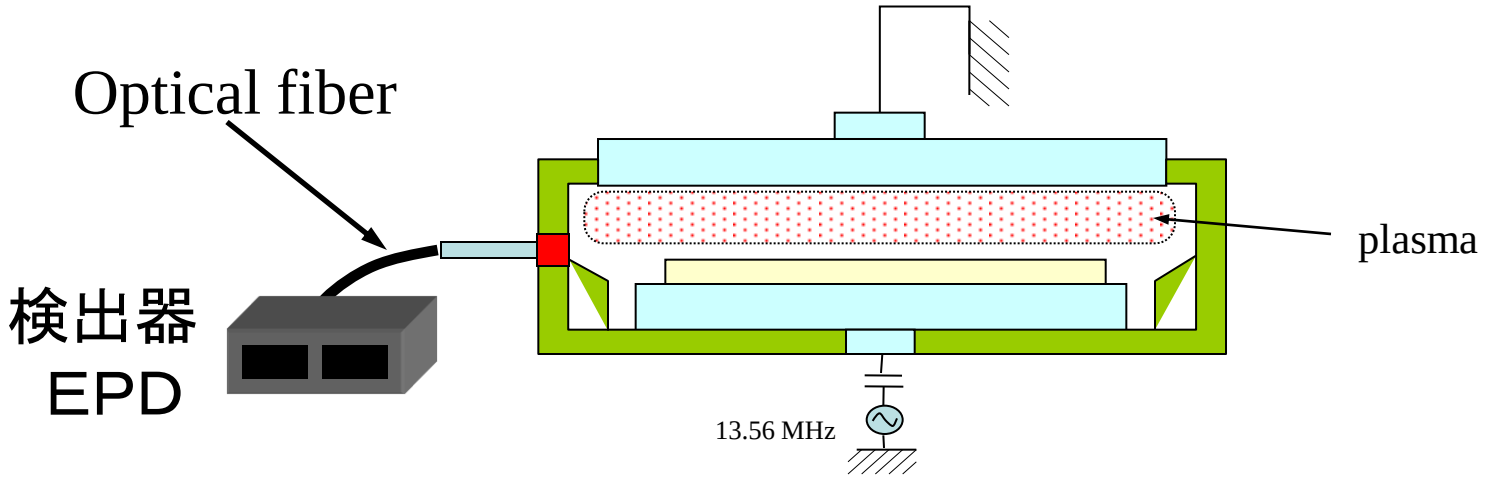
1. 目的

Dry Etching 蚀刻终点检测。

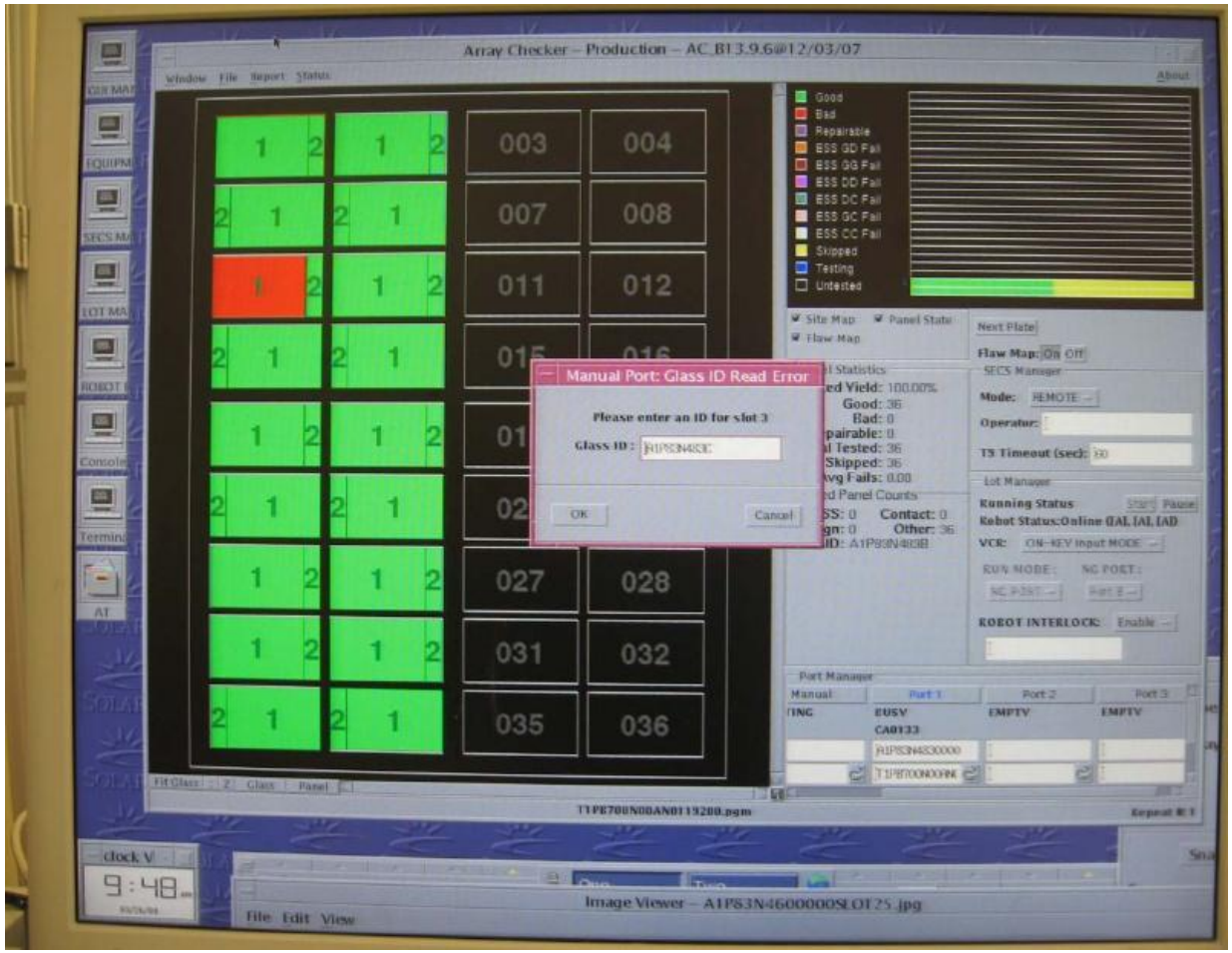
End Point Detector

2. 原理

利用从蚀刻中开始到结束为止特定的波长的光强度的变化，检测出蚀刻的最合适的终点。

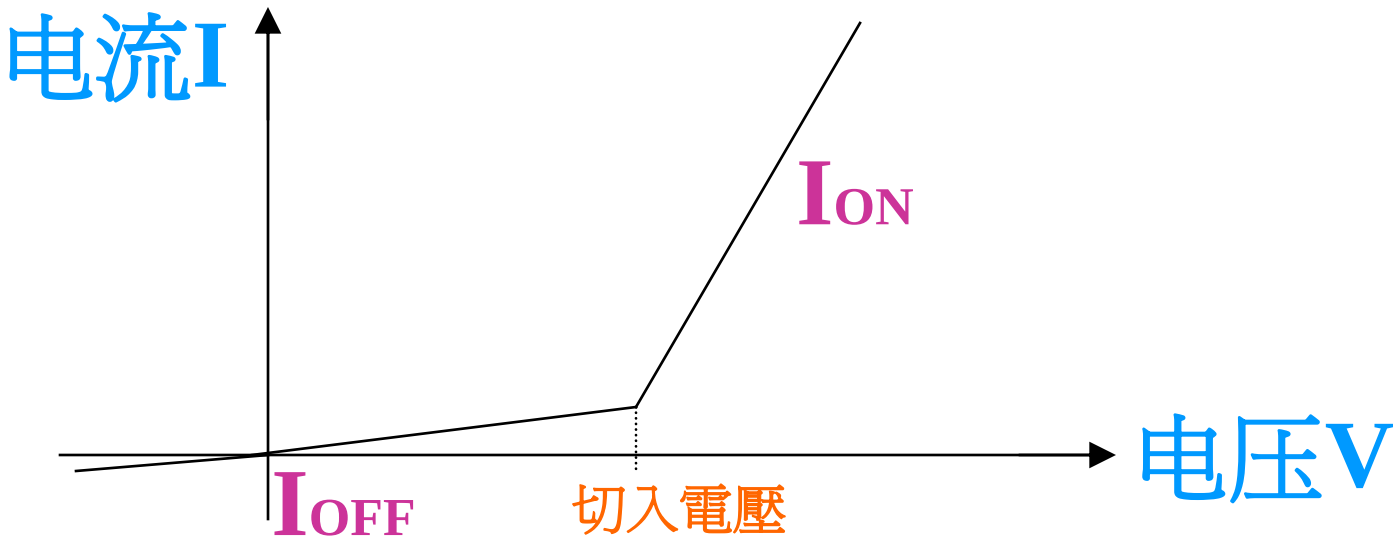


Array Tester



将TFT Array Panel进行测试，如果有短路（SHORT),或是短路(OPEN),就将坐标点记录下来，传给Laser Repair（激光修复机）修复之

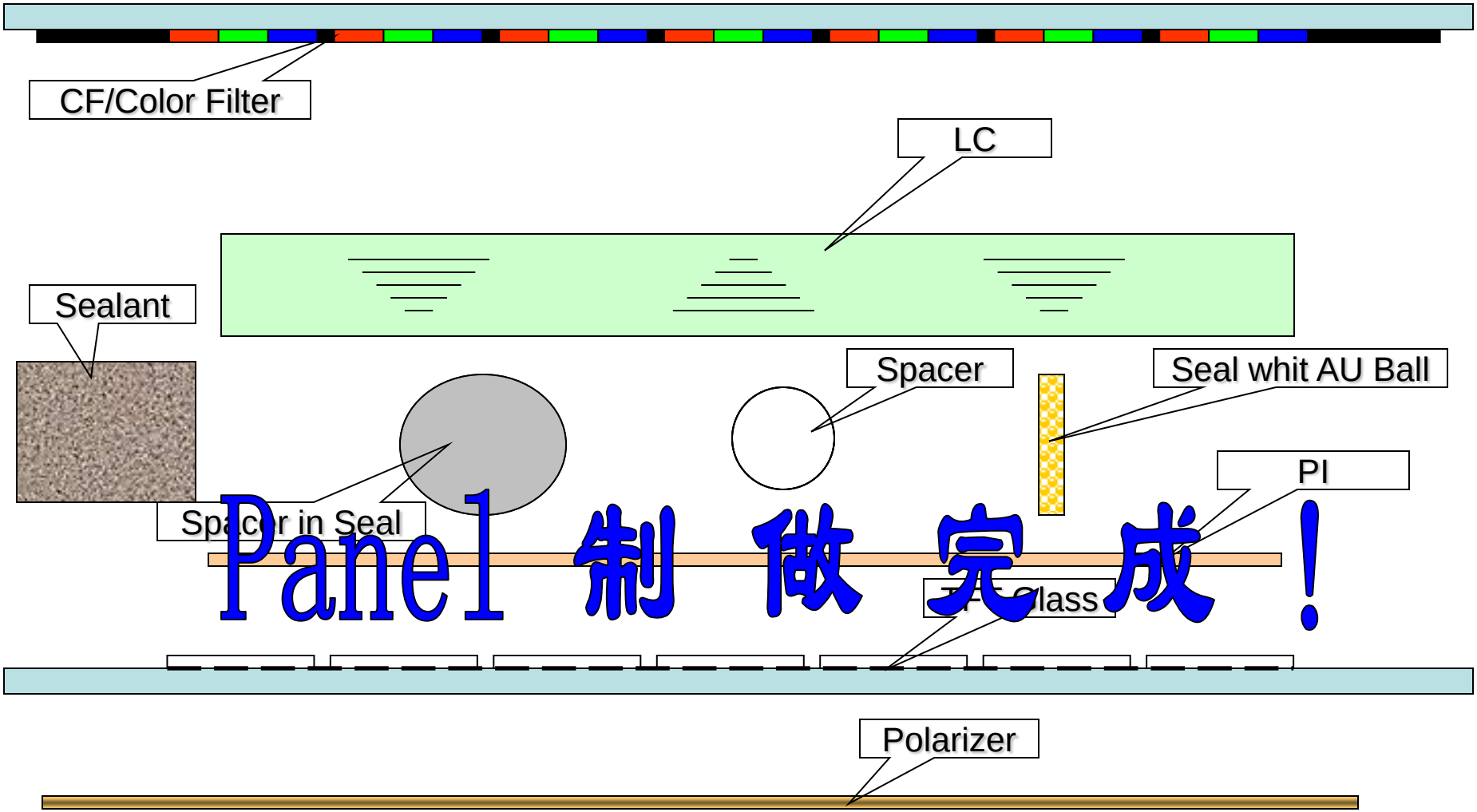
1.测量元件导通电流,I_{ON}
2.测量元件截止电流,I_{OFF}
3.测量切入(CUT IN)电压V_T
4.测量电压电流曲线TV CURVE



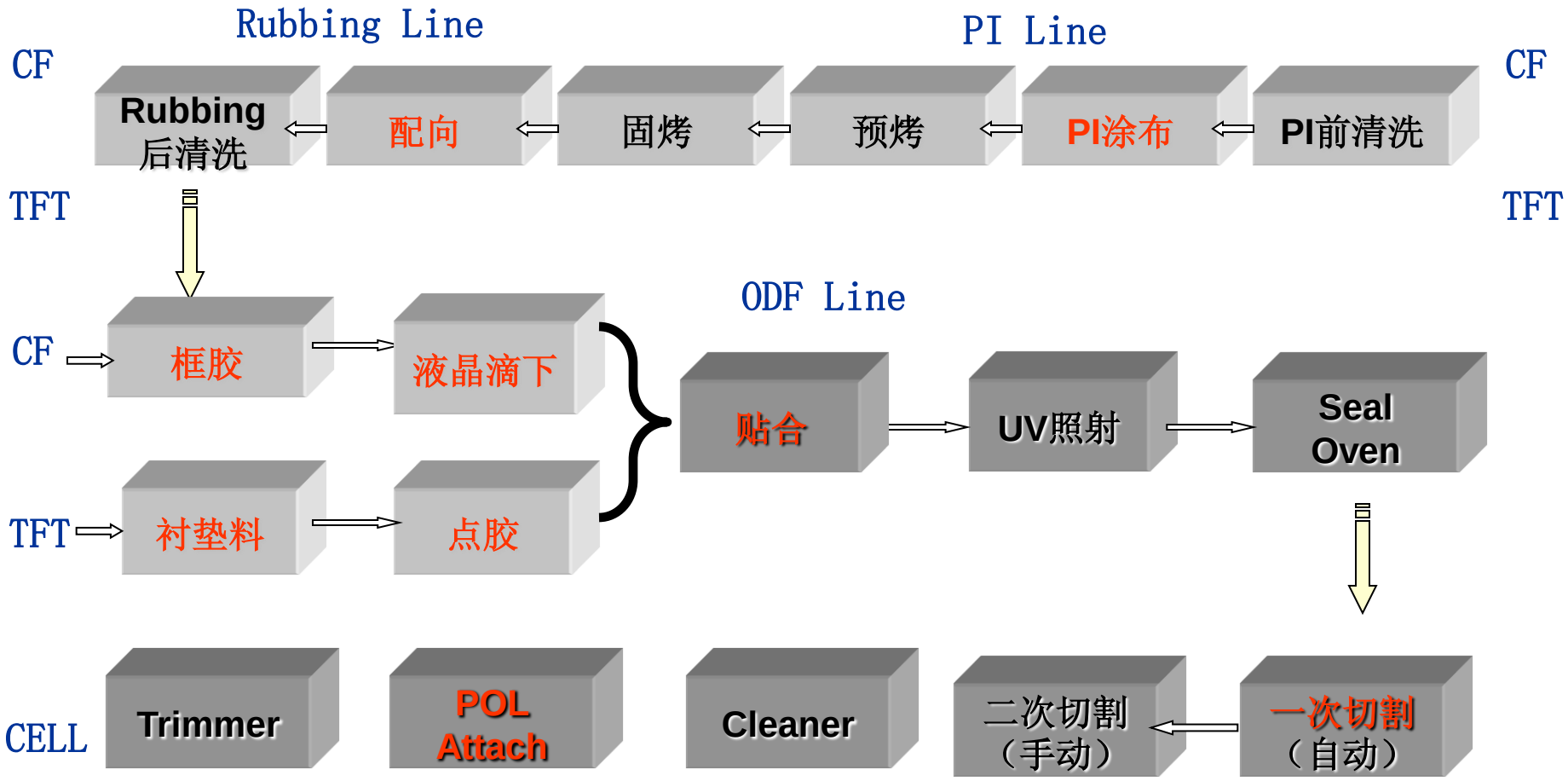
QUESTION AND ANSWER

TAKE A BREAK

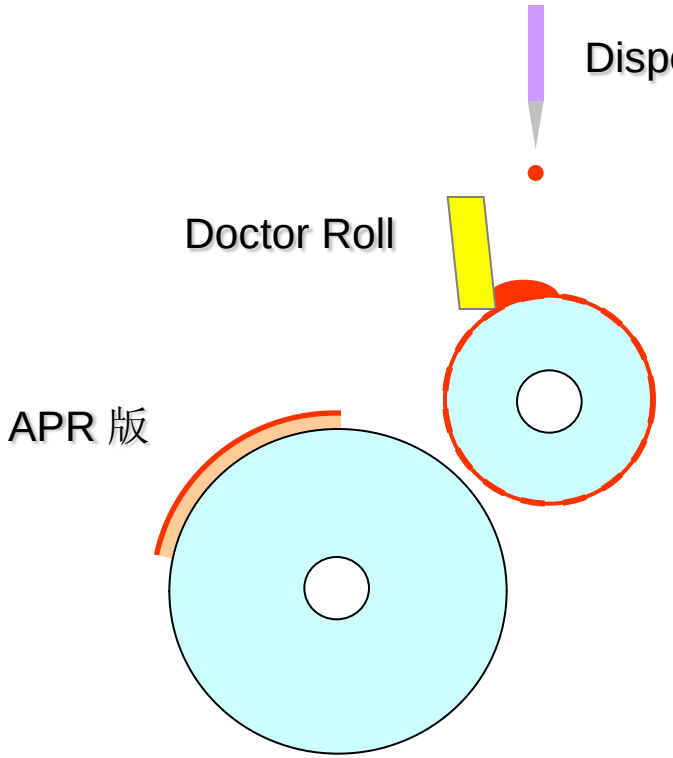
二：Cell Process



CELL工艺流程


Rubbing Line
PI Line
CF
CF
Rubbing
后清洗
配向
固烤
预烤
PI涂布
PI前清洗
TFT
TFT
ODF Line
CF
框胶
液晶滴下
贴合
UV照射
Seal
Oven
TFT
衬垫料
点胶
CELL
Trimmer
POL
Attach
Cleaner
二次切割
（手动）
一次切割
（自动）

PI Coater



Scraper Type

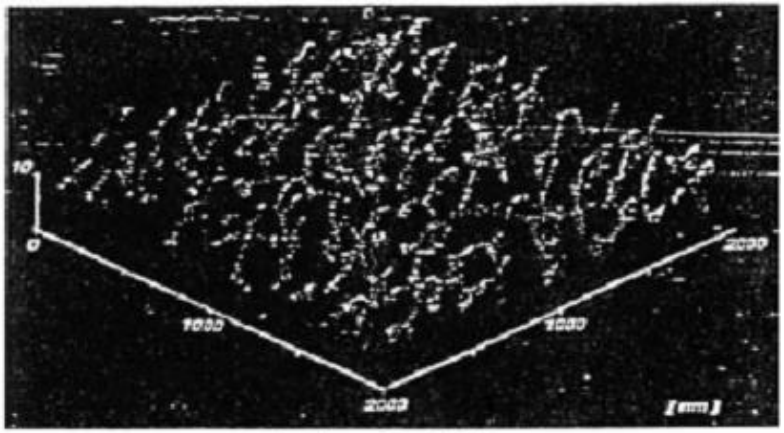
APR: Asahi Photosensitive Resin

PI Coater要求特性

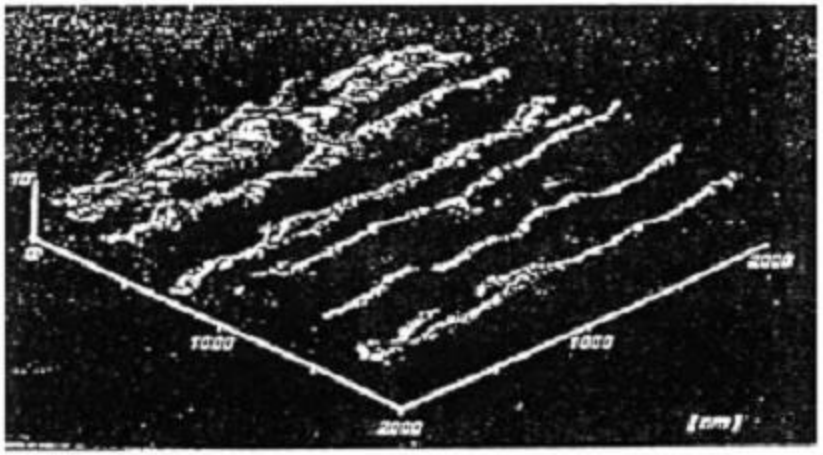
- 印刷性
- 與ITO接著性
- 膜強度
- 化學穩定性
- 耐熱性
- 配向性
- 低雜質
- 透明度
- 絕緣性
- 不產生靜電
- 高電壓保持率
- 沒有殘留影像
- 信賴性
- 低環化溫度

Process

Rubbing

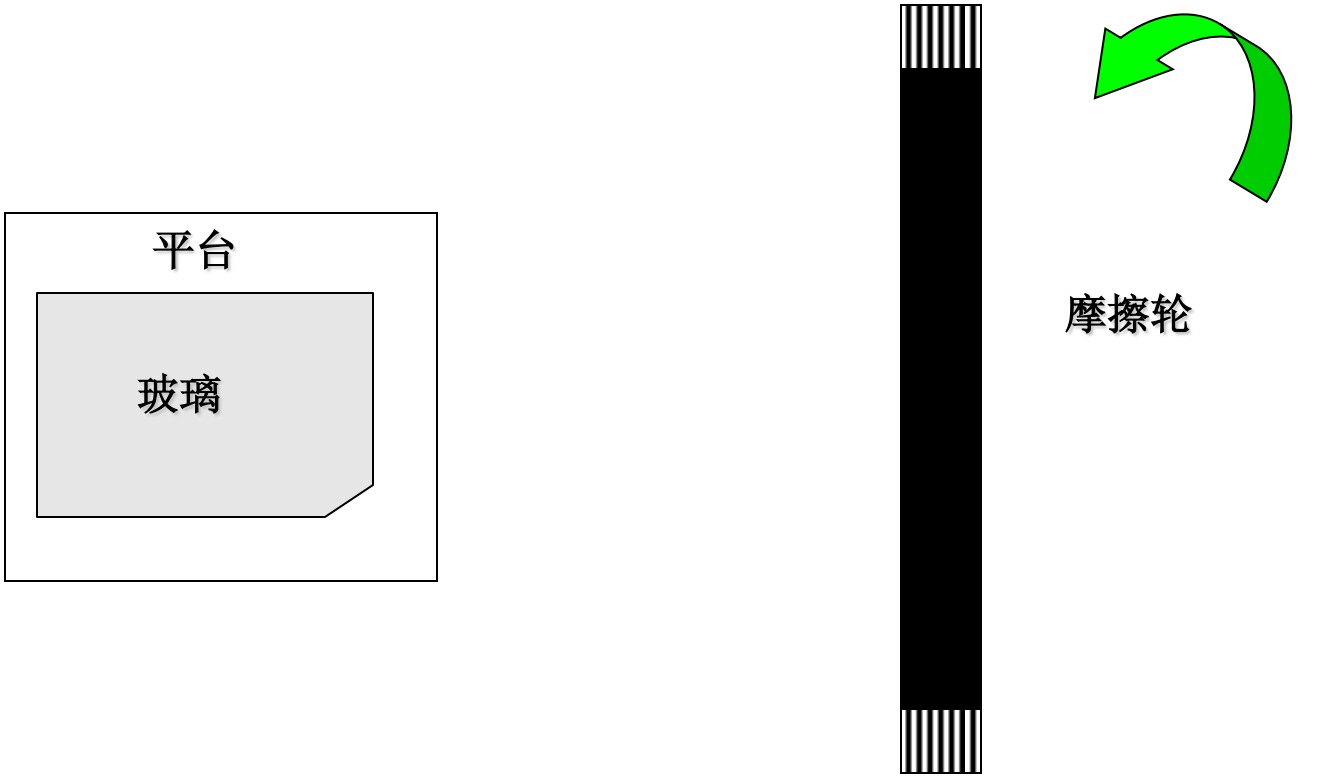


Before Rubbing



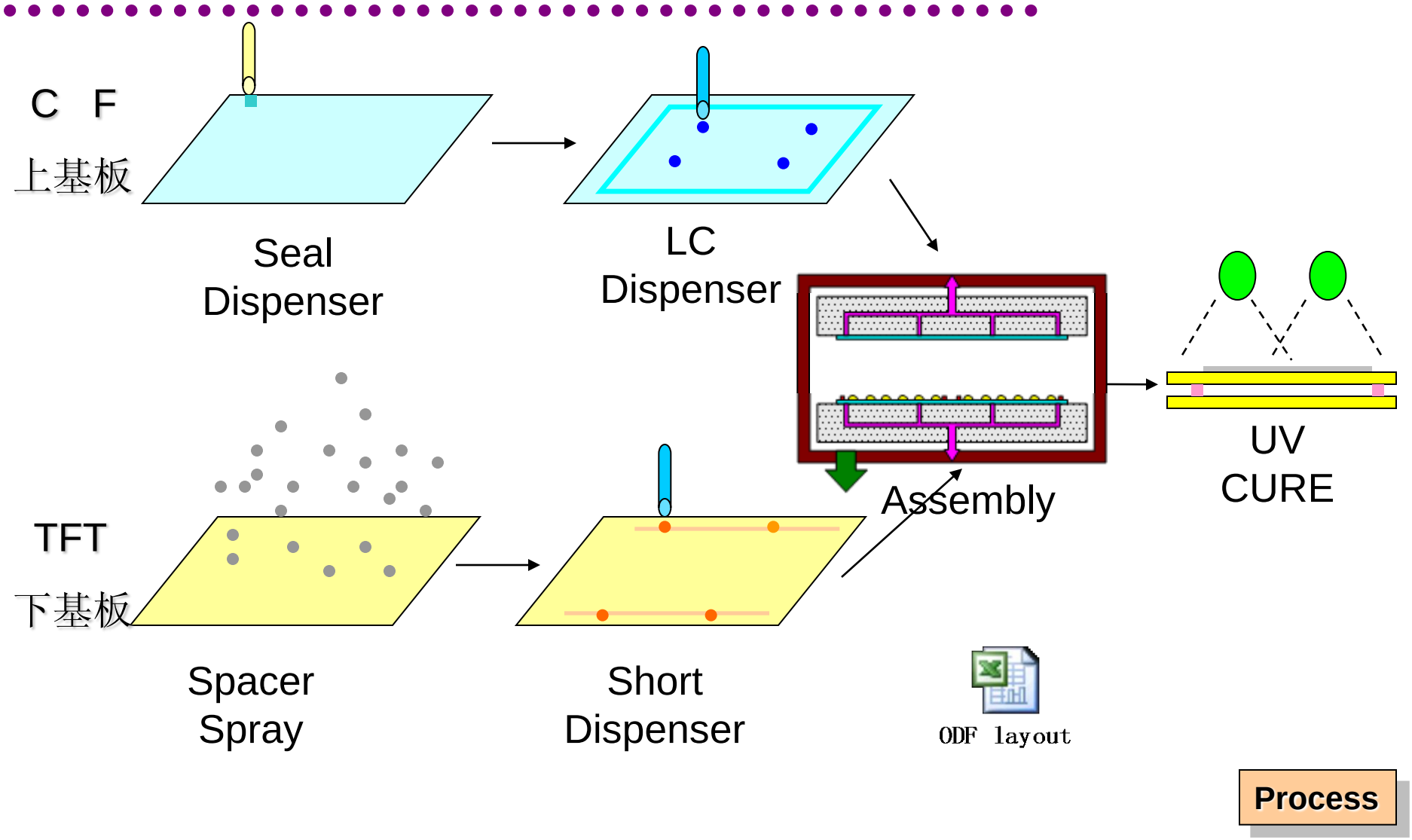
After Rubbing

Rubbing 动作



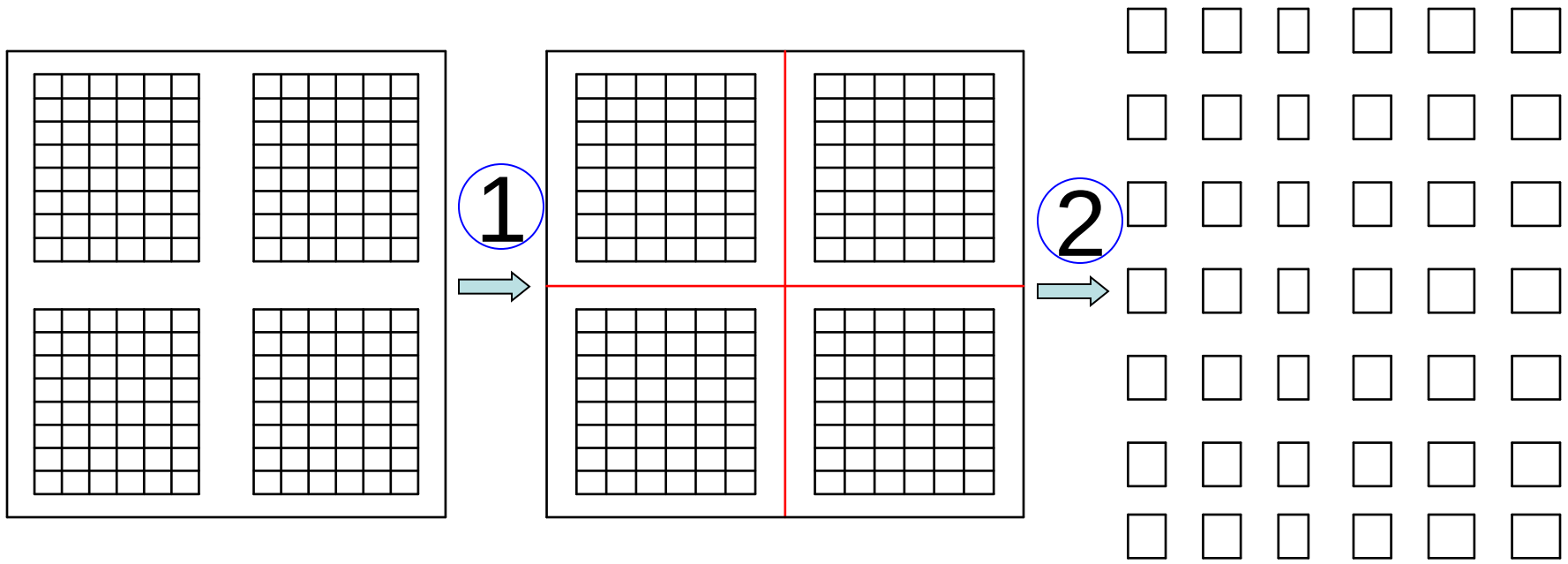
Process

ODF制成



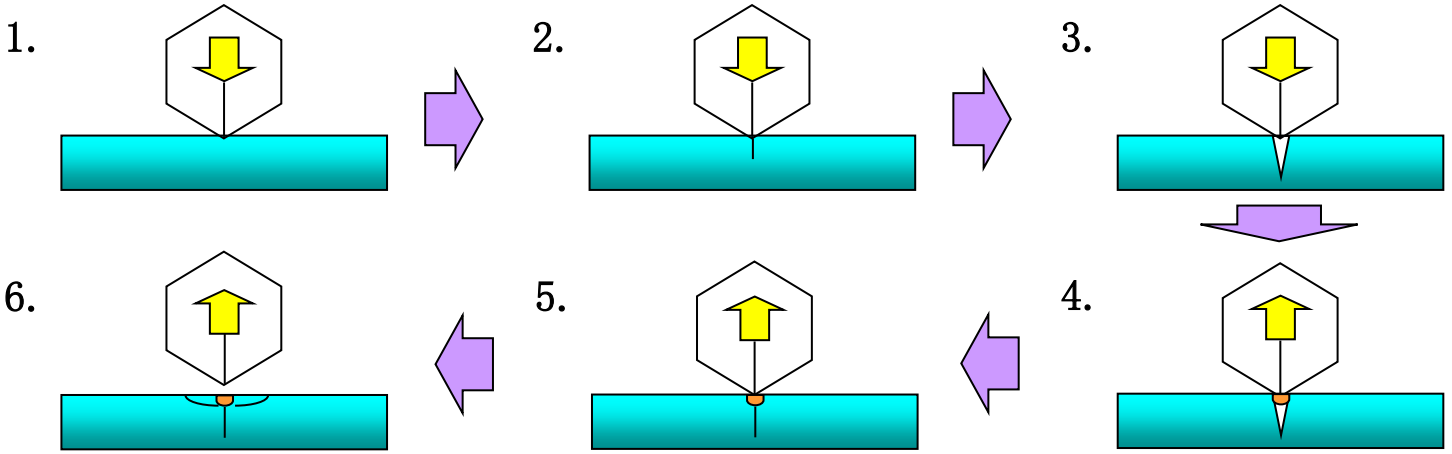
Process

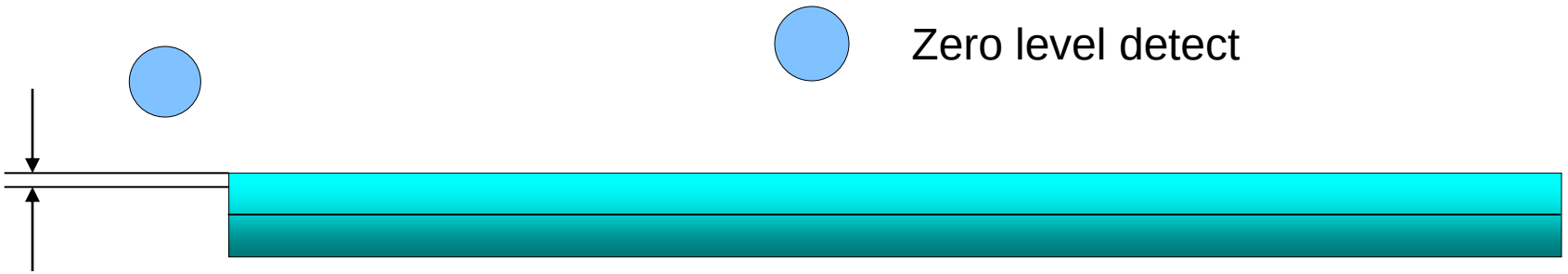
Scriber



Process

切割过程

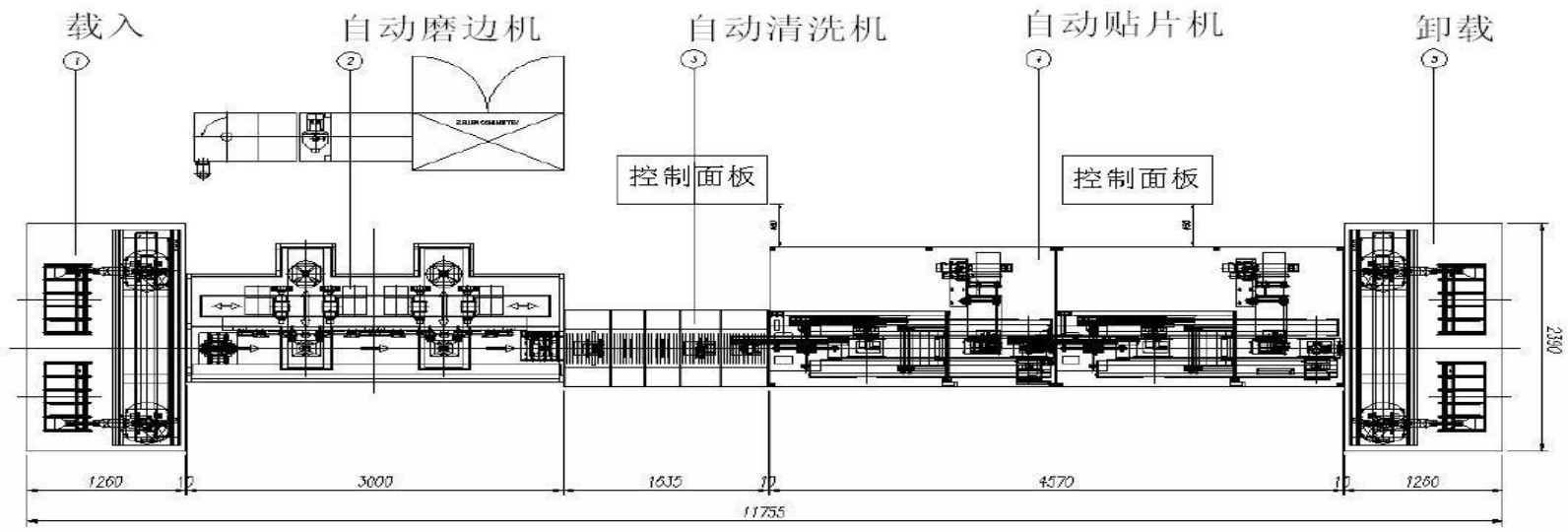




工作台运动方向及速度

Process

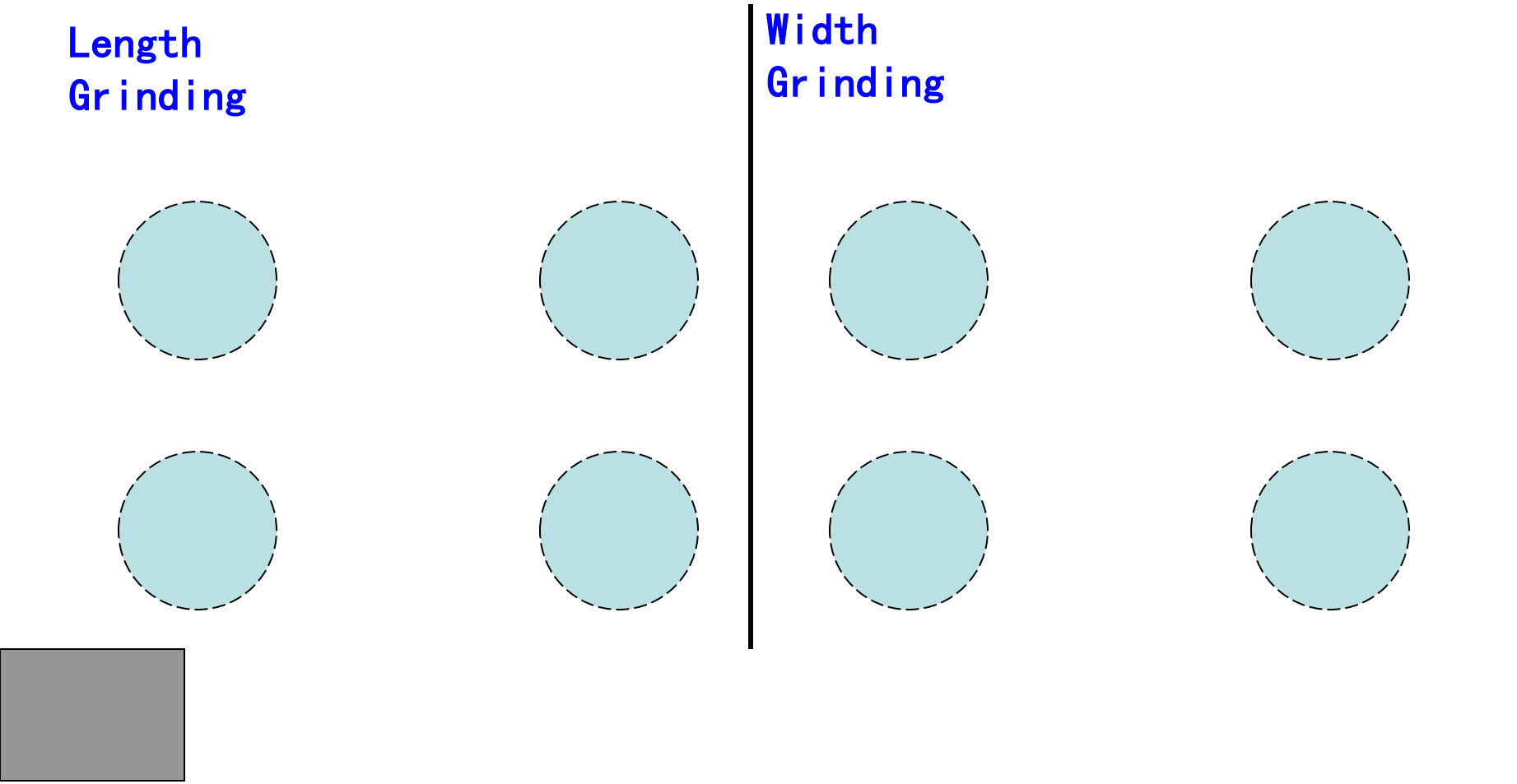
E-C-P


载入
自动磨边机
自动清洗机
自动贴片机
卸载
控制面板
控制面板
1260
10
3000
1635
10
4570
10
1260
11755
2350

Process

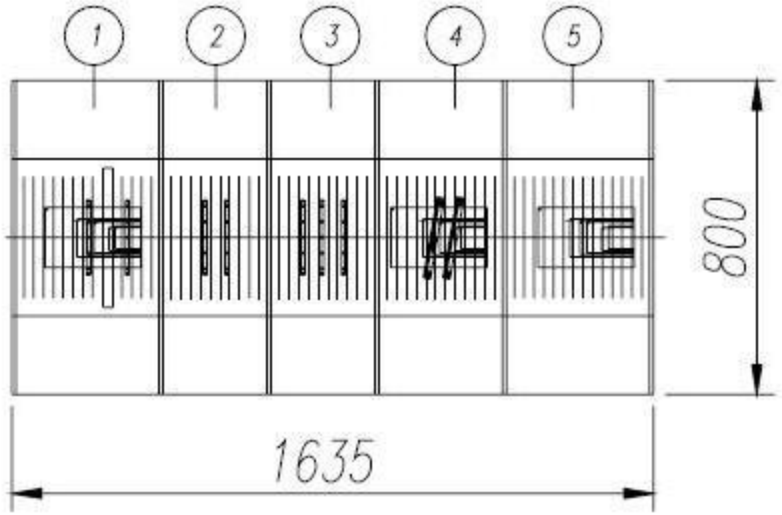
Edge Grind (Skip)

Process



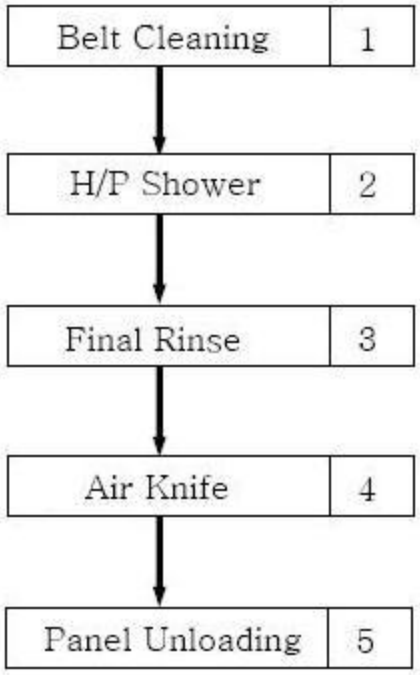
Cleaner

（1）基本构成



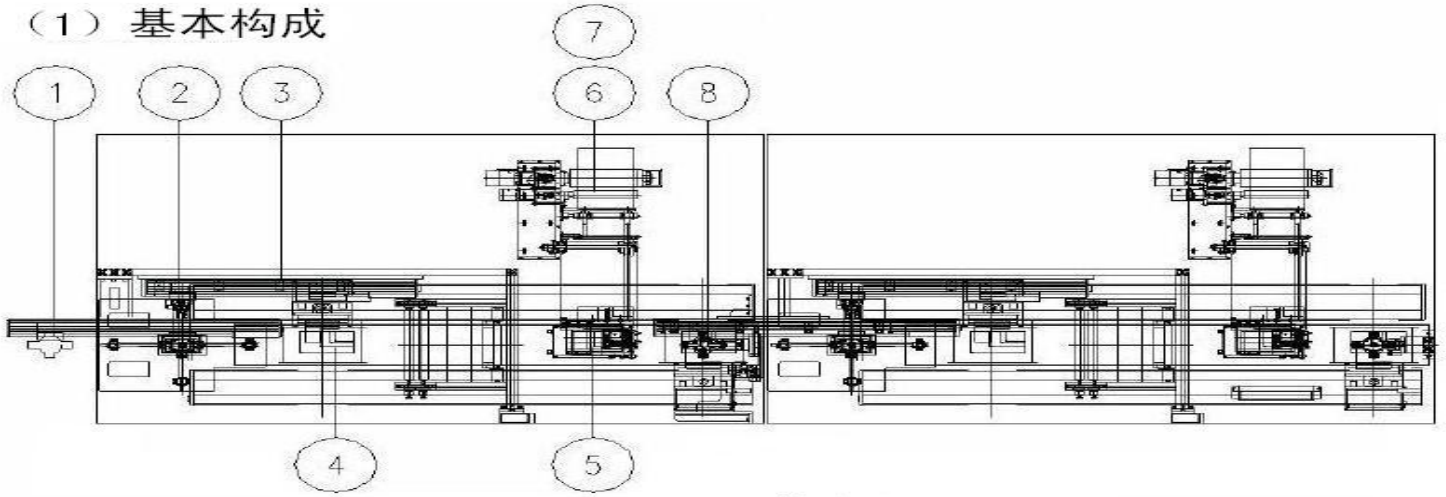
① BELT CLEANING ④ AIR KNIFE
② H/P SHOWER ⑤ UNLOADING C/V
③ FINAL RINSE

（2）工艺流程



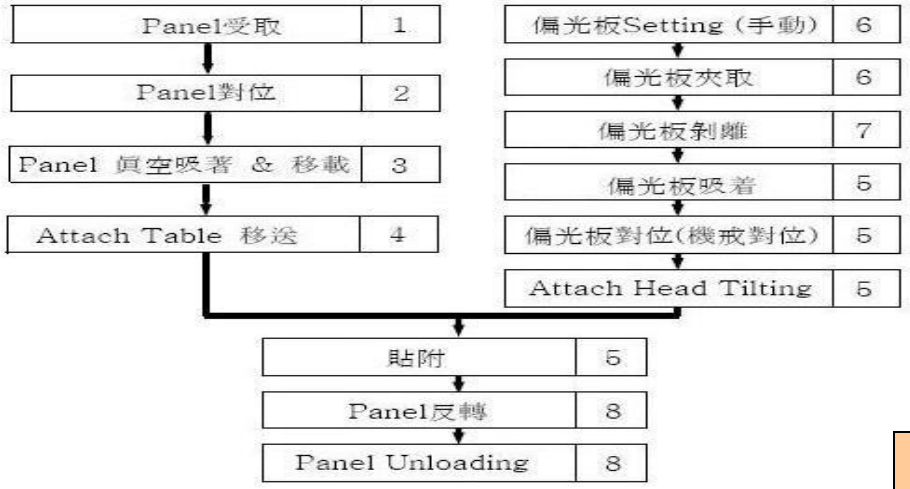
POL Attach

（1）基本构成



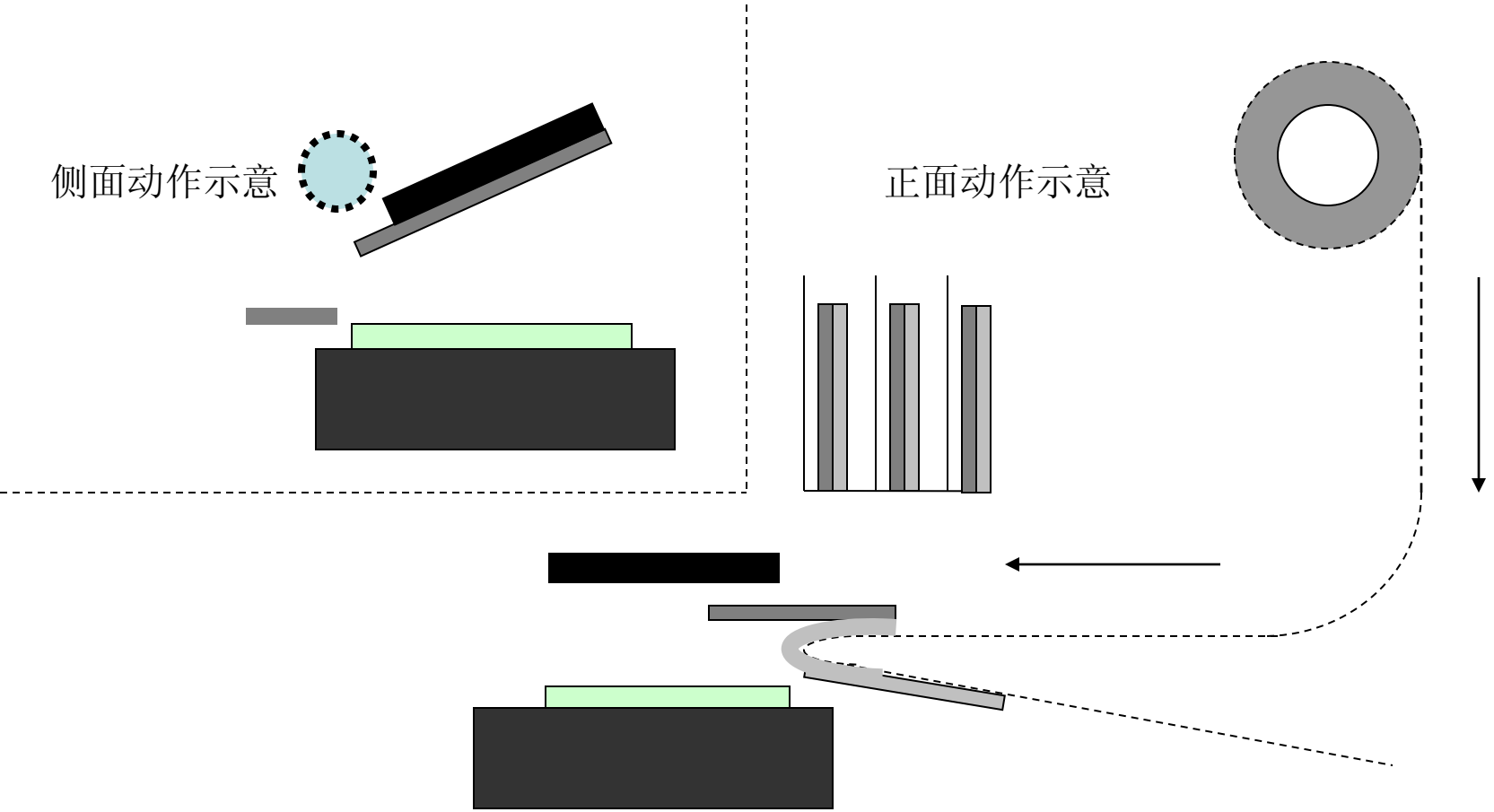
	UNIT NAME
1	PANEL PICK & PLACE
2	PANEL CENTERING
3	TABLE PICK & PLACE
4	ATTACH TABLE
5	ATTACH HEAD
6	POL MAGAZINE & SUPPLY
7	POL FILM DETACHER
8	PANEL TURN OVER

（2）工艺流程



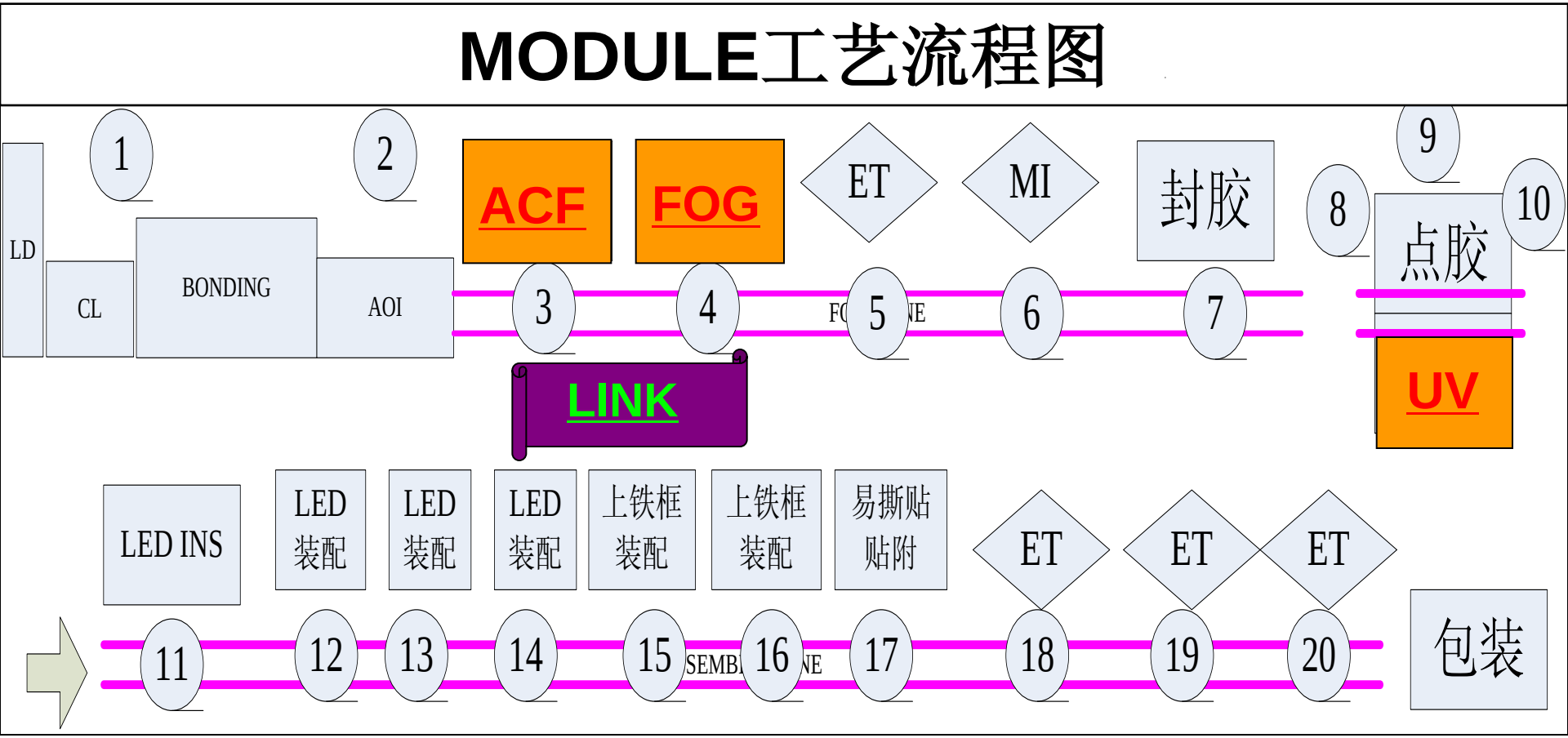
Process

POL Attach



Process

三：Module Process



Module Process Flow

COG	IC 邦定	
	□镜检	
	□AOI检测	
FOG	ACF 粘贴	
	FOG 邦定	
	□镜检	
	电测1	
	封胶	
	□胶带粘贴	
	补强	
	UV固化	
组装	□副屏电测	
	□背光源检测	
	□背光源组装	
	□主副屏焊接	
	□背光源焊接	
	□主副屏组装	
	□外框组装	
	□外框焊接	
	□触摸屏组装	
	□触摸屏焊接	
	□保护胶带粘贴	
	最终电测	
老化	老化	
包装	包装	
出货	出货	

JUMP

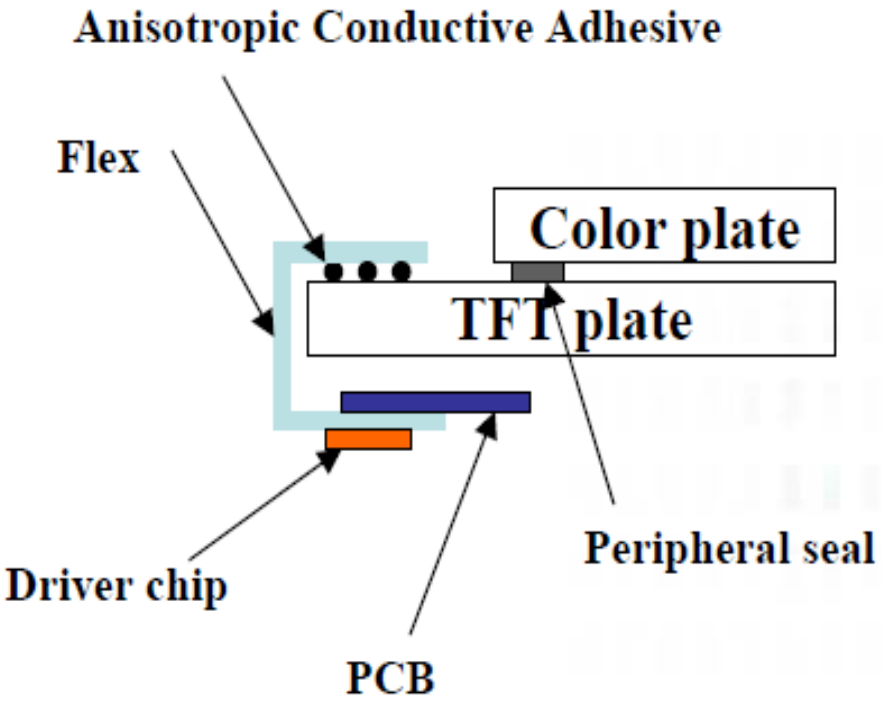
Driver Connection to Glass

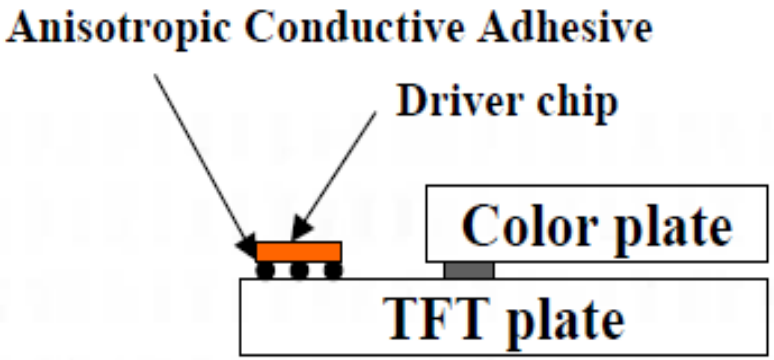
Chip on Film (COF) **or** **Chip on Glass (COG)**

TCP - Tape Carrier Package or

TAB - Tape Automated Bonding

Flip Chip



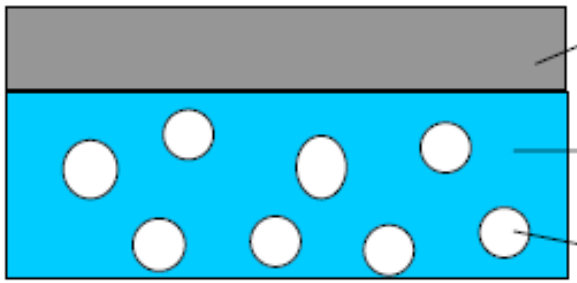


Poly-Si TFT LCD:
Drivers integrated on glass

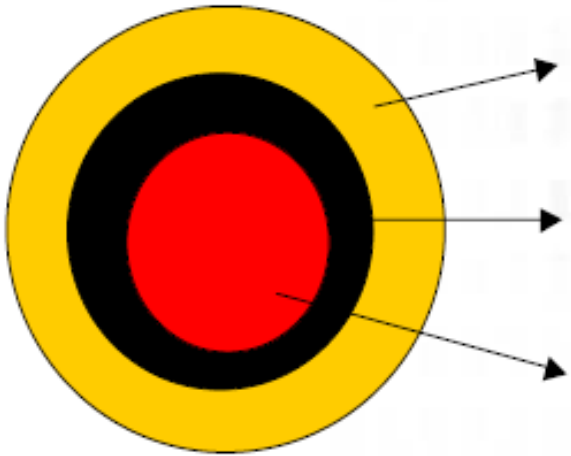
ACF (Anisotropic Conductive Film)

異方性導電膜

ACF structure



Conductive Particle structure



COG

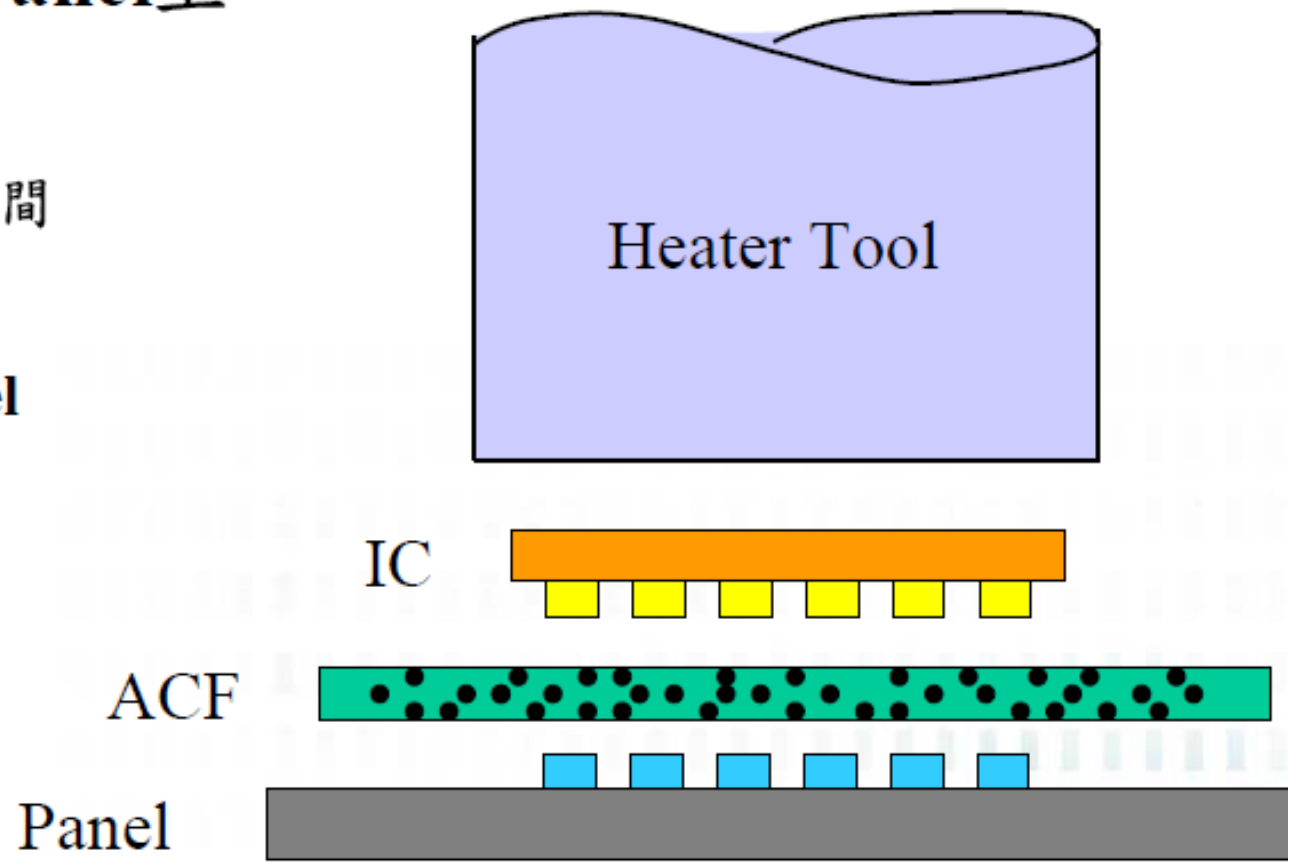
- 將IC壓著於Panel上

製程

溫度、 壓力 、時間

材料

ACF、IC、Panel



COG Process

ACF ATTACH

ACF 貼付於 Panel 上

↓

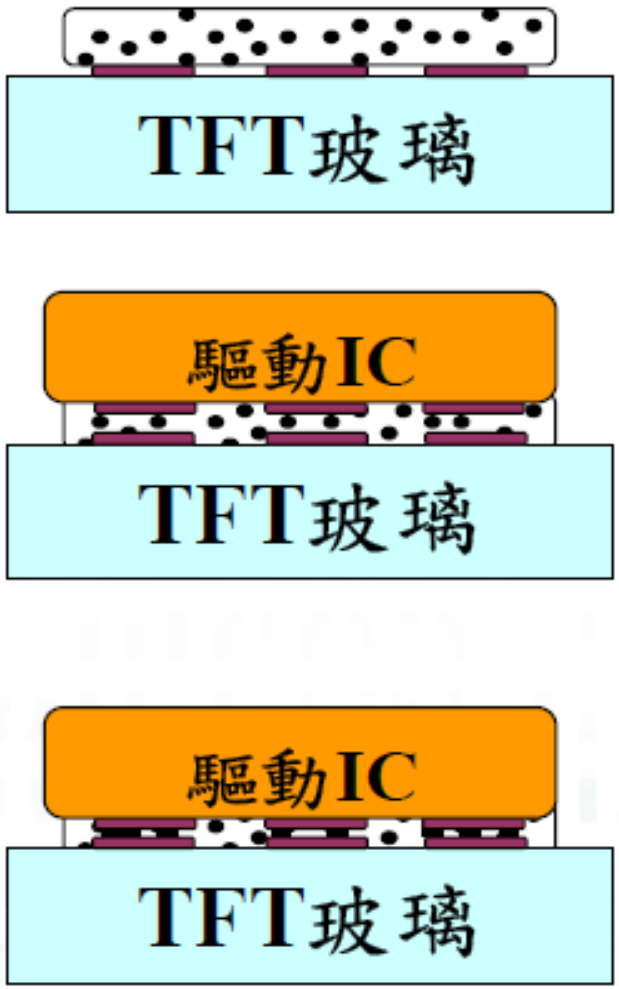
PRE-BOND

IC 對位 預壓於 Panel 上

↓

MAIN - BOND

高溫 高壓 IC 本壓於 Panel 上



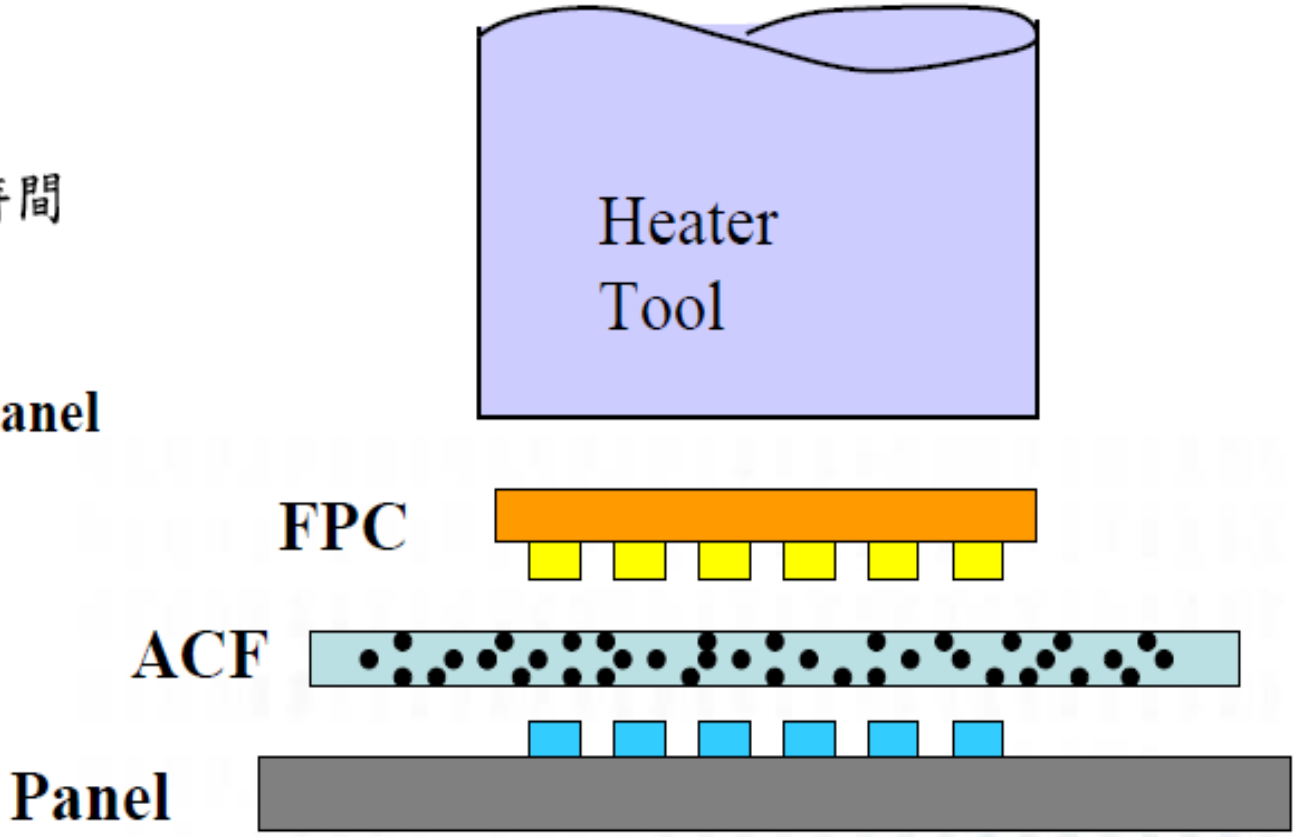
FPC (Flexible Printed Circuit)

- 將FPC壓著於Panel上

- 製程

  溫度、壓力、時間
- 材料

  ACF、FPC、Panel



FPC Process

ACF ATTACH

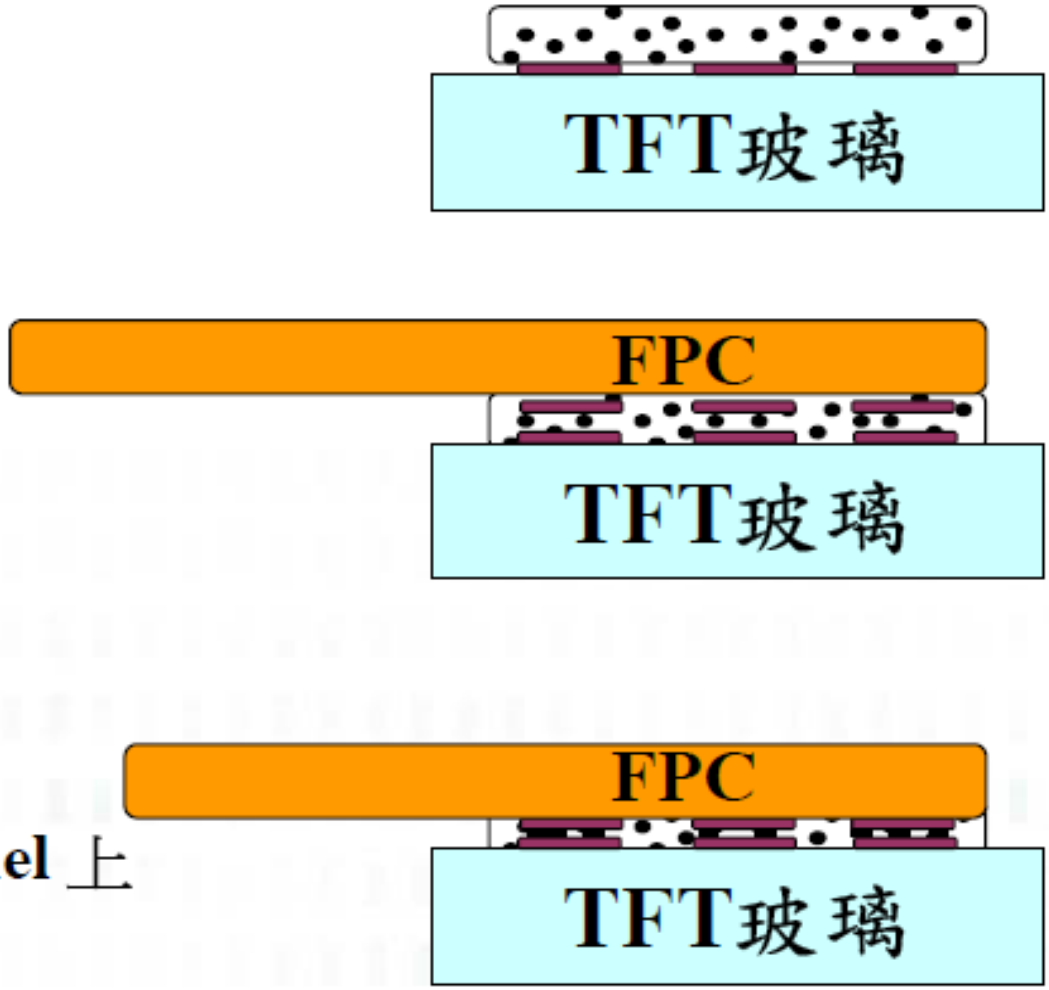
ACF 貼付於 Panel 上

PRE-BOND

FPC 對位 預壓於 Panel 上

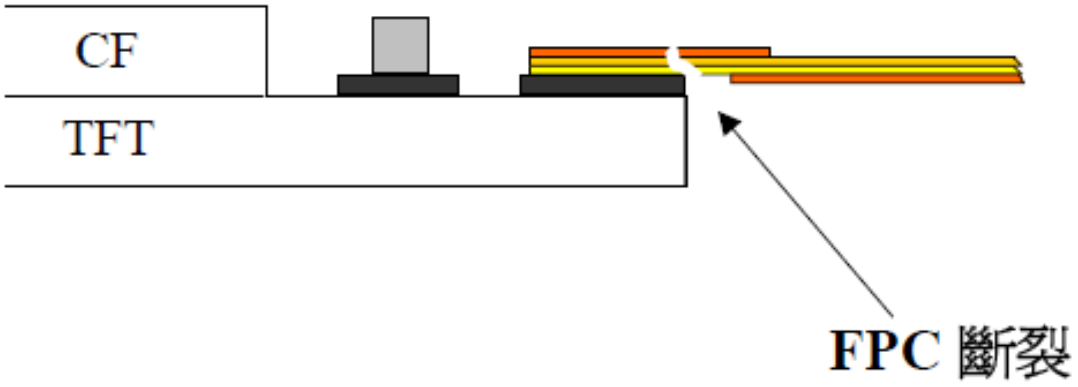
MAIN - BOND

高溫 高壓 FPC 本壓於 Panel 上



UV

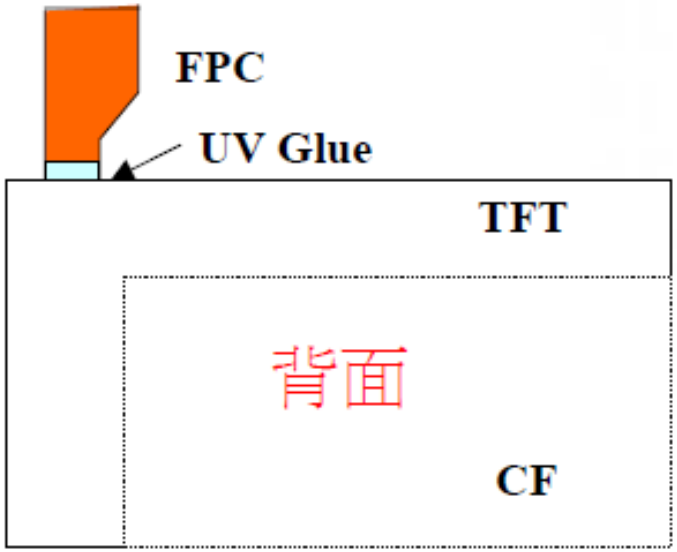
提供FPC與玻璃間的緊密接合增加FPC的抗拉強度，減少FPC斷裂所產生之不良.

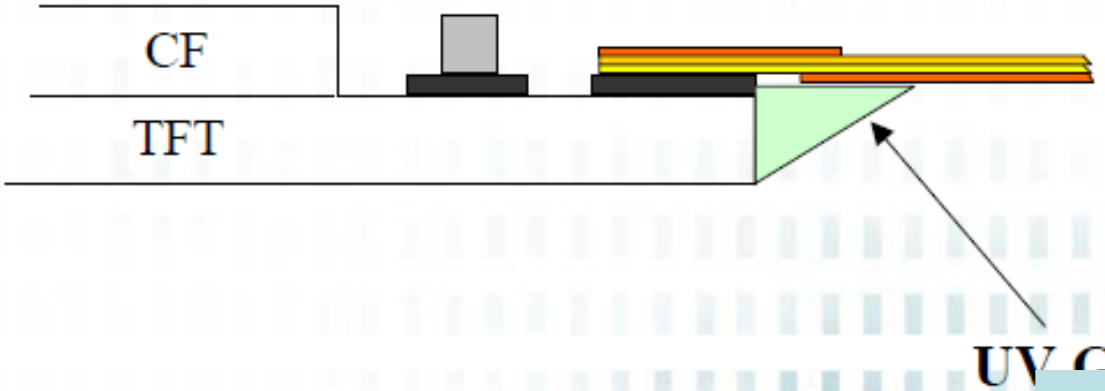


UV PROCESS

(1)UV 膠塗佈

(2)UV lamp 照射

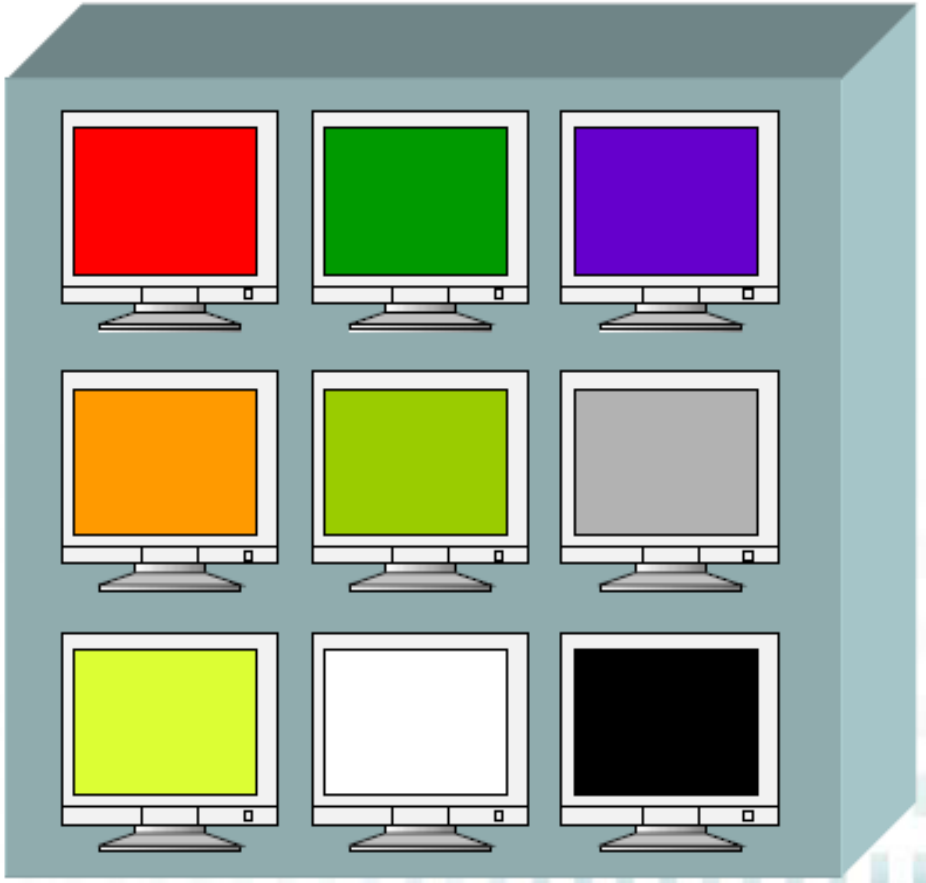




Aging

老化測試

- 壽命測試
- 穩定性測試



Aging Conditions:

50 deg. C

2 hrs

结束